A Survey of On-Chip Optical Interconnects

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Numerous challenges present themselves when scaling traditional on-chip electrical networks to large manycore processors. Some of these challenges include high latency, limitations on bandwidth, and power consumption. Researchers have therefore been looking for alternatives. As a result, on-chip nanophotonics has emerged as a strong substitute for traditional electrical NoCs.

As of 2017, on-chip optical networks have moved out of textbooks and found commercial applicability in short-haul networks such as links between servers on the same rack or between two components on the motherboard. It is widely acknowledged that in the near future, optical technologies will move beyond research prototypes and find their way into the chip. Optical networks already feature in the roadmaps of major processor manufacturers and most on-chip optical devices are beginning to show signs of maturity.

This paper is designed to provide a survey of on-chip optical technologies covering the basic physics underlying the operation of optical technologies, optical devices, popular architectures, power reduction techniques, and applications. The aim of this survey paper is to start from the fundamental concepts, and move on to the latest in the field of on-chip optical interconnects.

General Terms: Design, Performance

Additional Key Words and Phrases: Photonic networks, nano photonics, on-chip communication

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1. INTRODUCTION

The predominant discourse in the computer architecture community has changed significantly in the last decade. Instead of focussing on increasing the performance of individual cores, the community has endeavored to ensure that a chip as a whole maximizes instruction throughput. There is thus a strong emphasis on parallel and multi-programmed workloads, which have both computation and communication aspects. Since the cores are not necessarily getting any faster, the onus lies on the communication network to deliver performance gains. Secondly, due to continued scaling–which came about as a direct consequence of Moore's law– the number of cores has been doubling roughly once every two years, and will continue to do so till at least the next few years. Both these factors necessitate the development of a fast, responsive, and ultra-low power on-chip communication substrate.

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	Number of cores	Year
IBM Power4	2	2001
Sun Niagra	8	2005
Sony/Toshiba/ IBM Cell	9	2006
Azul Systems Vega 3	54	2008
Epiphany IV	64	2012
Xeon PHI	61	2013
TILE GX	72	2013
MIC Knight	72	2015

Fig. 1. Number of cores per multicore chip (not considering GPUs here)

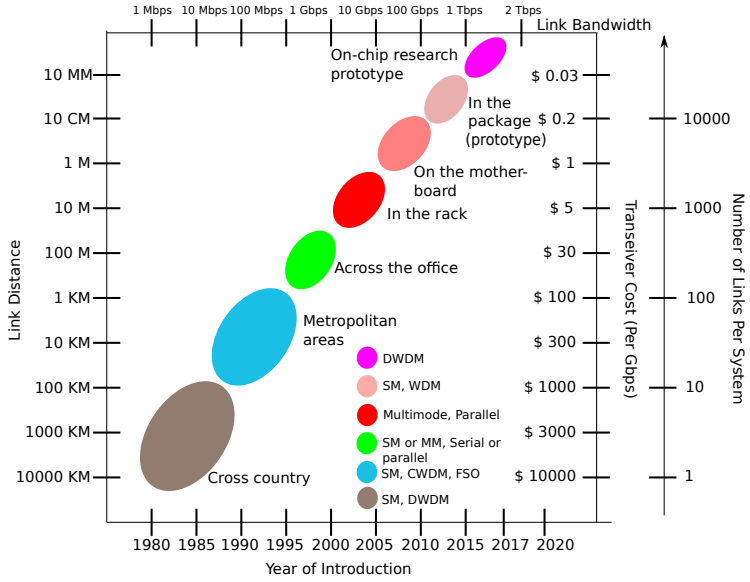

Fig. 2. Evolution of optical communication

Let us look back into the past, and note that when the number of components on a chip was modest(< 16) [Strauss et al. 2006], the elements were connected using a bus. But when the number of elements increased, researchers started proposing point to point electrical links. Thus, came the era of on-chip networks (NoCs) with fairly complex topologies.

An NoC (network-on-chip) provides a communication infrastructure that connects all the elements (cores, cache banks) of a chip. It consists of specialized routers that act as intermediate elements to route packets between sources and their destinations. The source node hands over the packet to its nearest router. The router decides the next hop based on the topology of the NoC and the routing algorithm. Because the number of cores and cache banks has been increasing exponentially, NoCs have increased in complexity. The latest mantra is *route packets not wires* [Dally and Towles 2001].

However, electrical NoCs have their limitations. Current trends indicate that 100+ cores will be housed on a single chip in the near future [Kurian et al. 2010]. Electrical NoCs will have scalability issues with such networks [Sikder et al. 2015], and with an increase in the number of cores (see Figure 1) on a chip, bandwidth will become the main bottleneck. Recent evidence [Zydek et al. 2008; Fujikata et al. 2008] suggests that electrical interconnects will not be able to provide high bandwidth while simultaneously maintaining acceptable levels of power, area, and performance.

As a result, the research community and industry are looking for alternatives. One promising alternative is on-chip nanophotonics (optical networks). Optical interconnects provide an opportunity to meet the demands of high bandwidth and at the same time help reduce power consumption, area, and delay of on-chip signals. The field is over 30 years old. The first paper on on-chip silicon photonics was published in 1984 by Goodman et al. [Goodman et al. 1984]. Subsequently, thousands of papers have been published in this area, including many from the computer architecture community.

Figure 2 shows how the optical communication bandwidth has changed over the years from 1980 to 2017. It also illustrates the length of the optical links, transceiver cost and the number of links per system. We observe that the development in the area of optical communication has been expeditious. Optical links have decreased from

thousands of kilometers to roughly 10 millimeters (on-chip links). The bandwidth has simultaneously increased from 1 Gbps to 1Tbps. The number of links in the system has also increased from 1 to 10,000. Optical networks have already come down to the level of the motherboard (Optical PCI-X [Intel 2013]), and the next logical step is for them to be used inside the chip.

There are various advantages of using optical communication over electrical communication. The main advantages are: data rate independent of distance, high bandwidth due to wavelength division multiplexing (WDM), reduced electromagnetic interference, fast signal propagation, and low power dissipation [Chen et al. 2004; Haurylau et al. 2006] [Kapur and Saraswat 2002; Kobrinsky 2004; Batten et al. 2008]. However, before they can be mass produced commercially, there are many technical hurdles that need to be crossed. We will discuss such issues in Section 3.4.

1.1. Motivation for this Survey

We are at a very interesting point in the development of optical networks. There is a lot of commercial interest in using optical networks to create next generation servers and data centers. A lot of this interest has been created in the recent years mainly because of the impending death of traditional Moore's law based scaling. There are three kinds of entities who are working on next generation photonics technology: hardware vendors, start-up companies, and academia.

Companies such as Intel [Review 2008; PLATFORM 2016; Photonics 2014], IBM [Research 2014] and HP [TECH 2014] are heavily invested in developing next generation photonics based solutions. Fujitsu recently released its Primenergy servers, where CPUs can communicate using photonics (based on Intel's Optical PCI-X technology). HP and Intel are working on futuristic server architectures referred to as The Machine and the Intel Rack Scale architecture respectively, where inter-CPU photonics is one of the main drivers. Some other companies such as Ayar labs [Labs 2015] and Luxtera [LUXTERA 2015] have a wide portfolio of photonics chips and communication modules. There is also extensive academic involvement in this area. For example, Sun et al. [Sun et al. 2015] have fabricated a processor chip containing 850 photonic components, which work together to provide an advanced NoC. Moreover, researchers at UC Berkeley [News 2015] have been successful in designing a 2-core processor based on photonic interconnects on an $18mm^2$ die.

The next logical step for industry is to have commercializable photonics based solutions inside a package and finally on the die. In this respect, academia is far ahead of industry in terms of ideas on how to use photonics components; hence, once the technology is available, the thoughts of academia and industry need to converge. We thus view this survey as very timely, because it summarizes most of the work done primarily in academia over the last 10 years. Engineers and researchers of tomorrow will hopefully find much of the content useful while developing practical photonics based solutions.

1.2. Organization of the paper

We start by providing some background related to photonics in Section 2, and then we subsequently look at the layered architecture of optical networks in the same section. We then start out by looking at optical devices in Section 3, and describe the key issues that are hindering their commercialization. We then look at optical architectures in Section 4, and then focus on one of the largest challenges for deploying optical networks, which is power consumption (in Section 5). We finally look at applications of optical networks in Section 6, and conclude in Section 7.

2. LAYERS IN AN OPTICAL NOC

In this paper, we shall study the design space of nanophotonic technologies and architectures by decomposing the space into four layers as shown in Figure 4. We devote one section to each layer, where we shall look at some of the seminal proposals, and their limitations. Before, we introduce our reference layered architecture and classification system, let us quickly provide an overview of the basic background of photonic architectures in Section 2.1.

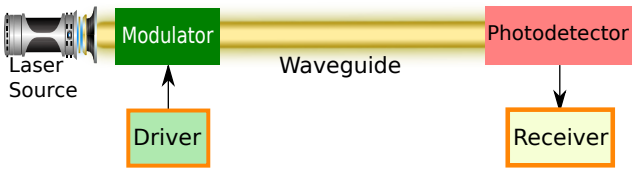

Fig. 3. A basic optical communication system

2.1. Basic Background

Figure 3 shows a typical optical communication system. First, we need a light source, which can either be an off-chip laser, or an on-chip laser. If the light signal is generated off-chip it needs to be brought into the chip with the help of special devices called *couplers*. Subsequently, *waveguides* are used to carry the optical signal around the chip. A waveguide is a slab of silicon or a polymer that guides light along its path. A waveguide used in photonics (on-chip optical communication) has a typical ribbed structure (typically 0.5-1μm wide and made of silicon).

The next step is modulating the optical signal to encode information. The presence of light at a time slot indicates 1, and absence indicates 0. Typically, a circular waveguide based structure called a *micro-ring resonator* [Barrios et al. 2003; Bogaerts et al. 2012] is used to modulate light. The micro-ring resonator can couple the light from a waveguide to another waveguide and remove almost all of the light to encode a logical 0. Alternatively, it is possible to take the resonator off resonance by applying a small electrical charge to it. This changes the refractive index of a portion of the circular waveguide, thus moving the resonator out of resonance. As a result, the optical signal is not removed from the original waveguide (logical 1). It is possible to do this billions of times a second, and thus encode a sequence of 0s and 1s.

To detect a signal at an optical station (transmitter + receiver), we need to first consider whether there are other stations downstream that might require the signal. If this is the case, then we need to use a beam splitter to split a fraction of the signal, and transfer it to another waveguide. A beam splitter can be created by forking the waveguide (Y-junction), or by using a directional coupler (two parallel waveguides). The signal then needs to be fed to a photodetector. The photo detectors at the end of the waveguides detect the amplitude of light and use a set of trans-impedance amplifiers to amplify the signal. The resulting digital signal can then be used by the rest of the circuit.

2.2. Optical Devices used in Photonic Networks

The lowest level in Figure 4 comprises of optical devices. At this level, the challenges (see Section 3) are mainly in the design and fabrication of components such as modulators, filters, couplers, and waveguides. We note that optical components are prone to manufacturing defects. Even a small amount of parameter variation such as imperfections in the fabricated design or operating temperature can significantly affect the

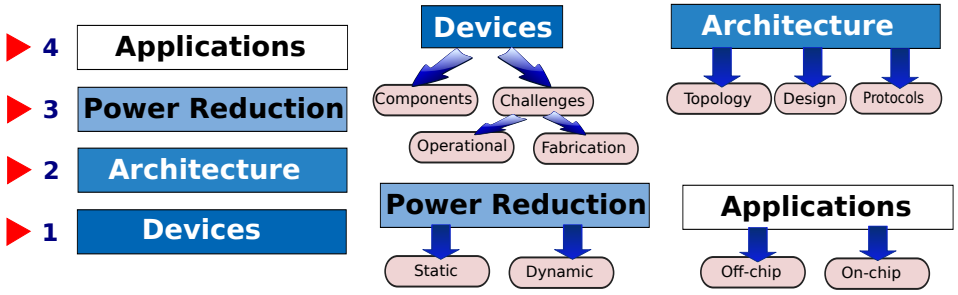

Fig. 4. Layers in an optical NoC

operation of the device. The nature of such variations and the steps taken to guarantee the normal operation of devices are a subject of this section. Some of the important steps that help in ensuring the normal operation of devices are thermal stabilization and compensating for parameter variations. Along with ensuring reliability, this section also discusses performance aspects of modern optical devices such as ultra-fast tunable splitters, GHz speed modulation techniques and power efficiency.

2.3. Optical Architectures

Subsequently, in Section 4 we discuss a spectrum of optical communication architectures. Specifically, we discuss different optical NoC topologies, the incorporation of different device technologies, and routing strategies. We first divide optical communication architectures into two types: 2D [Gu et al. 2009; Gu et al. 2008] and 3D [Ye et al. 2009]. 2D architectures typically have all their components embedded in one silicon layer. They can be arranged in many topologies such as a mesh or a torus. Similarly, 3D architectures [Morris et al. 2012; Ye et al. 2013] have many different topologies as well, which are conceptually very different from 2D topologies, because of the additional dimension.

We subsequently look at optical architectures based on the design and the communication framework that they use. They span from partially electro-optic networks [Bahirat and Pasricha 2009] to fully optical networks [Kurian et al. 2010; Kirman et al. 2006]. Different techniques in this spectrum have their pros and cons. To reduce the number of optical components, especially if there are manufacturing difficulties, it might be prudent to have a hybrid network where short distance communication is handled with traditional electrical networks. For some other designs based on the available technology and the nature of workloads, it might be wise to have *all-optical* networks.

Once the design, communication framework and topology have been decided, designers need to create a routing strategy to efficiently route packets between different points on the chip without incurring significant delays. Optical networks support both point-to-point links and large shared links with support for multicast traffic. The main challenges with point-to-point links is the need for buffering packets at intermediate nodes, setting up a path between the sender and the receiver, and routing packets from the sender to the receiver while minimizing latency. In the case of multicast/broadcast based shared links, the main challenge is power dissipation. Since optical losses are typically multiplicative in nature, it is very important to minimize optical power consumption. There are also issues with regards to arbitration in the case of shared channels. Sometimes a channel can be used by only one sender. It thus becomes necessary for the sender to arbitrate for the channel, and use the channel only after it has won the arbitration (gained exclusive access).

2.4. Power Consumption

After discussing optical technologies, and architectures, we shall look at an issue that is regarded as a major bottleneck in the commercial implementation and adoption of on-chip optical networks namely *power consumption*. Given the plethora of work in this area, we considered it necessary to add it as an additional layer in our reference architecture (see Figure 4). The physics of photons naturally constrains photonic architectures in the sense that photons cannot be stored; they need to be flowing all the time to carry information. To store the information carried in optical signals, either we perform expensive optical-to-electrical conversion, or we keep the laser on for most of the time, and ensure that photons are flowing through the waveguides whenever we want to send messages. Both these approaches waste a lot of power and can render photonic architectures infeasible. As a result most photonic architectures have a prominent power management component.

In Section 5 we shall look at the issues related to power consumption in optical networks and the techniques that researchers have proposed to minimize power consumption. The nature of techniques can be further sub-classified into two categories based on the nature of power dissipation: static power and dynamic power consumption. Static power consumption is by far the most dominant source of power consumption. The main source of static power consumption is the power loss due to the lasers staying on when no information is being sent. Thus, most techniques in this space are typically centered around modulating the laser or sharing the available bandwidth among transmitting nodes. Another type of static power consumption is the insertion loss. It refers to the power losses due to the non-ideal transmission efficiencies of components in the optical network.

Finally, the last source of static power consumption is the power required by small micro-heaters that ensure that the temperature of optical components such as ring resonators remains more or less constant.

Dynamic power consumption (due to data transmission and reception) takes place mainly due to the energy spent in O/E and E/O conversion, and the power consumed in transmitters and receivers.

2.5. Applications

Optical networks have primarily been proposed to handle regular NoC traffic such as directory-based coherence, searching for data in L2/L3 cache banks, and sending messages to the memory or I/O controllers. Other than such traditional applications, specialized applications of optical networks are few.

The proposals for using optical networks for other applications can be subdivided into two categories: off-chip and on-chip. Off-chip uses of optical networks include interacting with memory modules, and the DMA controller. Similarly, in the last few years several novel applications of on-chip photonic networks have emerged. Some of the uses are implementing fast barriers, arbitration mechanisms, synchronization primitives such as locks, snoopy based cache coherence, and NUCA (non-uniform cache access) protocols for large L2/L3 caches. We shall discuss such applications in Section 6, leading to the observation that we mainly use the low latency of optical networks and their inherent multicast capabilities to implement such features.

3. OPTICAL DEVICES USED IN PHOTONIC NETWORKS

The goal of this section is to provide an overview of some of the major components used in on-chip optical communication systems (for a deeper discussion refer to the paper by Miller et al. [Miller 2009]).

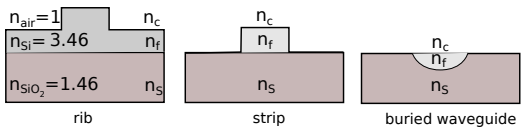

Fig. 5. Different types of waveguides

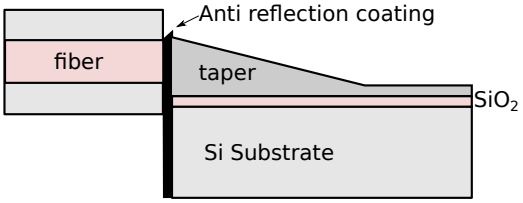

Fig. 6. Taper

3.1. Light Sources: Laser

Most lasers are built around a simple principle: stimulate a material to produce light, and then amplify it such that the final output signal is coherent. This material is known as the *gain medium* and is fundamental to a laser. A gain medium can be stimulated to produce light by injecting electrical charge, or by transmitting an optical signal through it. Most lasers place the gain medium between two optical mirrors. As light bounces between these mirrors, it stimulates the gain medium to produce more light using the photoelectric effect. One of these mirrors is slightly translucent, and some of the light leaks out from the cavity (region between the mirrors). This light forms the output of the laser. There are different methods of forming an optical cavity, and stimulating the gain media to produce light. We can thus make many different kinds of lasers.

(1) DFB (Distributed Feedback) Laser [Plumb 1989; Faugeron et al. 2012; Faugeron et al. 2013]: It is a single frequency laser diode, which is commonly used in optical communication. A diffraction grating is etched close to a p-n junction. It is a weak reflector and is spread all over the gain ridge (edge of the gain medium). This grating provides the required feedback for lasing. The wavelength is determined by the pitch of the grating and it can vary with changes in temperature. Such a DFB laser has a broad spectrum and is extensively used in fiber-optic communication.
(2) DBR (Distributed Bragg Reflector) Lasers [Aral 2005]: This is the quintessential laser that consists of a gain medium between two optically reflecting surfaces. One of these mirrors is made of a diffraction grating that reflects only one wavelength (the lasing wavelength). DFB lasers are almost always preferred in this class of lasers.
(3) MQW (Multiple Quantum Well) Laser [Meyer et al. 1995; Selmic et al. 2001]: In a quantum well laser, the optical cavity is very small. As a result quantum effects set in and the energy levels get quantized. Since distinct energy levels form, it becomes possible to achieve lasing by stimulating the gain medium. MQW lasers can be very small; however they are difficult to manufacture.
(4) VCSEL(Vertical Cavity Surface Emitting) Laser [Michalzik and Ebeling 2003; Syrbu et al. 2008]: VCSEL lasers are small enough to be integrated on-chip. Here, the axis of the optical cavity is oriented along the direction of the flow of current, in stark contrast to conventional lasers, where these axes are perpendicular to each other. This feature confers some unique advantages as compared to other lasers in terms of area efficiency. Unlike other lasers, the optical signal is emitted in a direction that is perpendicular to the orientation of the laser. As a result we only pay the price (in terms of area) of the cross-sectional area of the laser, and we can thus integrate thousands of such lasers on a chip. A useful analogy would be a city with tall skyscrapers. Along with the possibility of integrating many thousands of such lasers, VCSEL lasers also have higher yield rates – a vital requirement in today's nanometer scale fabrication processes.

3.1.1. On-chip and Off-chip Lasers. Let us now look at on-chip and off-chip lasers.

Off Chip Lasers:

The gain medium of an off-chip laser is typically made of silicon doped with III-V materials such as Gallium and Arsenic, or it is made of Erbium doped silicon that makes use of the Raman effect. To support DWDM (dense wavelength division multiplexing) we need to produce light at multiple wavelengths (typically 64 [Vantrease et al. 2008]). This can either be done off-chip with a multi-wavelength source, or can be done on-chip with comb based splitters [Levy et al. 2011], which can split monochromatic light at 1550 nm to produce light at 64 different equispaced wavelengths.

Subsequently, the laser needs to be coupled to a waveguide inside the chip using special tapered waveguides [Peng et al. 2010] (trapezoid shaped waveguides). The optical power is then distributed to the individual optical stations using a dedicated set of waveguides known as *power waveguides*.

The disadvantages of an off-chip laser are as follows. The first is that it has a relatively lower *wall-plug efficiency* as compared to other competing technologies. The wall-plug efficiency is defined as the ratio of the generated optical power to the input electrical power. An off-chip laser's wall-plug efficiency is roughly 20% today [Bai et al. 2011] and is expected to rise to about 30% [Bai et al. 2011] over the next few generations. Secondly, it needs to remain turned on most of the time. Sending a signal to modulate an off-chip laser is typically time-consuming. Hence, if we turn a laser off to save power, we need to wait for a long time (hundreds of ns) to turn it on again. The main benefit of long intra-chip optical networks is low latency and we shall cease to acquire this benefit if we incur this delay.

Here, it is important to mention another category of lasers called DML lasers (directly modulated lasers) that can be modulated very easily. For such lasers, it is possible to directly modulate the output of the laser (at GHz speeds) by varying the electrical power input. These lasers are commercially available (examples: Finisar DM 80, Emcore Medallion, Fitel FOL15DDBA), and have been fabricated by many research groups as well [Faugeron et al. 2012; FAUGERON et al. 2013; Huang et al. 2008; Burie et al. 2010; Faugeron et al. 2013]. The crucial issue in designing DML lasers is thermal stability. The response of a typical laser directly depends on the temperature of the gain medium. As a result switching it on and off frequently is difficult because it takes time for the media in the laser to reach the desired temperature. However, designers of DML lasers have to a large extent been able to address such issues. A naive approach is to ensure that the laser is operated always at a constant temperature using either micro-heaters or thermo-electric coolers. However, in 2010, uncooled DML lasers were demonstrated. They have shown stable operation till 100°C at 25 Gbps [Fukamachi et al. 2010]. Furthermore, it is possible to create a tunable laser source with multiple power levels by using an array of DML lasers (Peter et al. [Peter et al. 2015]).

On Chip VCSEL Lasers:

In comparison to off chip lasers, VCSEL lasers can be integrated on chip. They consist of two parallel Bragg reflecting surfaces with a quantum well in the middle. Each VCSEL laser can typically produce 3-10 mW of optical power. Hence, we typically need to use an array of VCSEL lasers to generate strong optical signals. VCSEL lasers have relatively higher wall-plug efficiencies, and can be modulated at GHz frequencies [Amann and Hofmann 2009]. Wall-plug efficiencies of VCSEL lasers are around 30% today, and are expected to go up to 50% over the next decade [Amann and Hofmann 2009; Seurin et al. 2009]. Instead of using ring resonators, we can directly modulate the lasers electrically.

However, VCSEL lasers have their set of problems. The first is that since they are integrated into the chip, their power dissipation gets added to the on-chip power. This further stresses the already stressed heat dissipation system of the chip. In the case of off-chip lasers, we can afford to dissipate a lot of power off chip.

3.2. Signal Propagation: Waveguides

A *waveguide* is considered as the basic building block of an on-chip optical network. Waveguides are channels through which light passes in an optical network. The working of a waveguide is based on the concept of total internal reflection. It is made by coating a high refractive index material (called core) with a relatively low refractive index material (called cladding). This structure helps to confine the light within the high-refractive index material and does not allow the light to escape. High refractive index silicon and low refractive index polymers such as siloxane polymer [Tanahashi et al. 1995] are the popular choices for the material used in the fabrication of the core of a waveguide. SiO_2 or siloxane polymer doped with TiO_2 [Tanahashi et al. 1995] is commonly used for the cladding layer.

From the point of view of performance, polymers are a better choice because they have a lower refractive index ($\approx$1.3) than silicon, and thus light travels faster within them. However, polymer waveguides are not used frequently because of the difficulty in fabricating modulators for such waveguides. Additionally, the bandwidth density (number of wavelengths that can be carried) of silicon waveguides is much better than polymer waveguides. This gives us more opportunities for dense wavelength division multiplexing with silicon waveguides.

We show the design of the three major types of waveguides (based on the position of the core and cladding) in Figure 5. Out of these the ribbed waveguide is considered to be the most efficient (in terms of power loss) [Vivien et al. 2005]. Waveguides need not be confined to one layer. However, it is possible to have multi-layer optical architectures. We typically need optical TSVs (through-silicon vias) [Killge et al. 2016; Yu et al. 2016] to connect waveguides across layers. The Optical TSVs are designed to enable the light to pass through different silicon stacks in a 3D chip. They are usually made up of a silicon dioxide cladding layer and a polymer based core with a higher refractive index than the cladding [Parekh et al. 2011].

3.2.1. Tapers. Typically off-chip waveguides (or fibers) are much wider than on-chip waveguides. Coupling light from a wider waveguide to a narrower waveguide is difficult given the fact that there is a high chance for light to escape. Directly coupling two waveguides with different radii can lead to high coupling losses($\approx$20dB) [Heck and Bowers 2014]. The solution is to use tapers[Birks and Li 1992; Almeida et al. 2003] (as shown in Figure 6). A taper is a trapezoid shaped structure that couples light between waveguides with different radii. Specifically, in Figure 6, the silicon dioxide layer should be at least $1\mu m$ thick, and an anti-reflection coating is required to avoid Fresnel diffraction.

3.2.2. Bends. A waveguide bend is used to implement a turn in a waveguide. It is sophisticated enough to be classified as a separate structure particularly because it is associated with large signal losses [Rahman et al. 2008]. At the waveguide bend, because of a change in direction, power is lost because of the conversion of the type of the signal propagation from a guided mode to an unguided mode. This loss strongly depends on the nature of the bend – whether the bend is a gradual curve or made up of a sequence of curves. A full wave simulation of a 90° bend with Synopsys RSoft is shown in Figure 10. Note that the main parameters of a waveguide bend are its inner radius, outer radius, rib width, rib height, and etch depth, and they determine the signal loss.

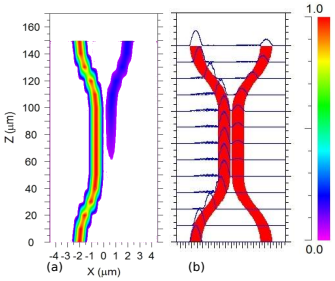

Fig. 7. Directional coupler

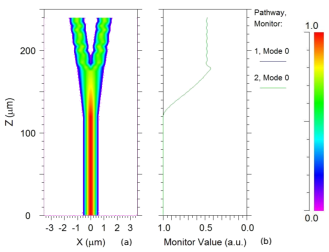

Fig. 8. Y junction

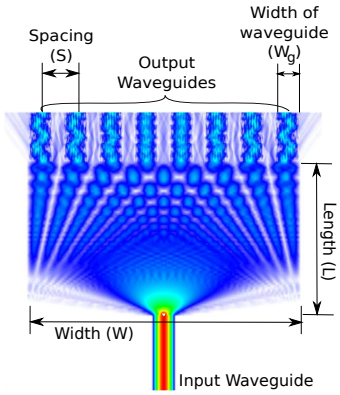

Fig. 9. MMI

3.2.3. Couplers/ Beam Splitters. Power splitters (also known as beam splitters) and couplers are the optical devices in on-chip networks, which are used to transfer a certain fraction of optical power from one waveguide to another waveguide.

Different kinds of beam splitters are used in on-chip optical networks. Examples of some devices are: directional coupler [Somekh et al. 1973; Bergh et al. 1980], Y junction [Yajima 1973; Izutsu et al. 1982], AWGR [Yin et al. 2013], and MMI [Peter and Sarangi 2014]. By changing the dimensions of these structures or their optical parameters, splitters can be fabricated with different split ratios. Currently, there are splitters available that can change the split ratio dynamically also [Peter et al. 2016]. They can be manufactured with MMI based devices [Zhou and Kodi 2013] or ring resonators[Peter et al. 2016].

Directional coupler. The Directional Coupler (DC) (see Figure 7) is a set of two parallel waveguides kept in close proximity. When the optical signal pass through one waveguide, the evanescent parts of the guided modes overlap and some energy gets transferred to the parallel waveguide. The energy transfer takes place recursively for a few times before it settles to a steady-state level.

Y junction. The Y junction is an optical structure where one waveguide splits into two. It can be used either as a splitter or as a combiner. If the device splits the signal into two equal parts, then it is a symmetrical splitter. It can split the signal asymmetrically also. The signal loss at a Y junction depends on the size of the tip and the opening angle (refer to the RSoft simulation of a Y-junction as shown in Figure 8).

AWGR. Arrayed Wavelength Grating Routers (AWGR) are mainly used in on-chip optical networks to multiplex a large number of signals from several waveguides into one combined signal. The combined signal is then sent through a single waveguide and at the other end these routers act as demultiplexers and separate out the original signals. This type of multiplexing and demultiplexing increases the overall transmission capacity of the network.

MMI. MMI stands for Multimode Interference Coupler, and is most commonly used as a broadcast element. A $1 \times N$ MMI device splits the optical signal into N parts, where each part is a copy of the original with a reduced amplitude. The light enters the MMI, undergoes diffraction and then gets reflected off the walls of the MMI device. The reflected waves constructively interfere to form high interference spots. The light gets coupled into the output waveguides, which are placed at these interference spots. Unfortunately, an MMI is a very fragile structure, difficult to fabricate, and is

very sensitive to process variation. Furthermore, MMI devices are heavily restricted in terms of fanout.

3.3. Modulation: Microring Resonators

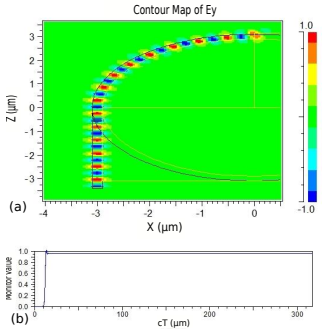

Fig. 10. Bend

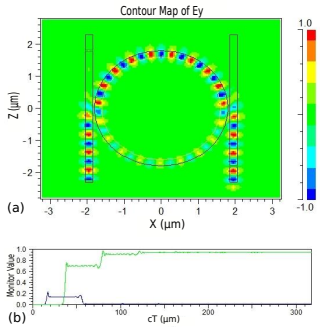

Fig. 11. Microring resonator

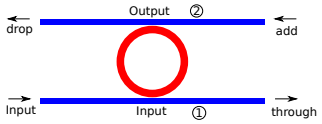

Fig. 12. Schematic diagram of microring resonator

A microring resonator is a combination of two straight waveguides and a circular waveguide placed side by side as shown in Figure 12. The signal enters waveguide 1 via the input port, and if the structure is not in resonance then the signal leaves through the through port of the waveguide 1. However, by applying a small electric change, it is possible to change the refractive index of the waveguides to bring the structure into resonance. In this case, light couples into the circular waveguide, and leaves through waveguide 2 via the drop port. Gradually, over time the amount of signal that gets coupled from waveguide 1 to waveguide 2 via the circular waveguide increases till almost the entire signal gets removed from waveguide 1. This is the point of resonance. Note that it is possible to take the resonator off resonance by slightly modifying the refractive indices of the waveguides. This can be done by applying a small amount of electrical change, or by a change in the temperature.

A ring resonator is primarily used to modulate light on a waveguide because it has the capability to either remove 100% of the signal, or keep all of it flowing in the waveguide. A microring (or ring) resonator basically performs electrical to optical (E/O) conversion. The delay due to the use of microring resonators for E/O conversion is found to be around 200ps [Xu et al. 2005]. In addition, it is also used in optical switches to transfer signals from one waveguide to another. A ring resonator is a fairly delicate structure, and is very sensitive to the wavelength of light. It can, thus, also be used to selectively transfer signals belonging to a certain wavelength. In Figure 11, we show the full wave simulation of a microring resonator in RSoft. Light enters the structure through the waveguide in the left, and then the coupled signal travels within the ring till it gets coupled with the output waveguide completely.

The other method of modulation is to use the Mach-Zehnder Interferometer(MZI). It is an optical device that divides the light into two parts, induces a phase shift in one part by changing the refractive index of the waveguide and then allows the two parts to recombine. The recombination may be constructive or destructive depending upon the phase shift induced by the MZI. A phase shift of 180° is induced if we want to encode a logical 0, otherwise a phase shift of 0° is induced for encoding a 1. One such modulator based on MZI was demonstrated by Liao et al. [Liao et al. 2005] with a bandwidth of 10GHz. It supports a data transmission rate from 6Gbps to 10Gbps.

3.3.1. Receiver. At the receiver, we need 3 components to detect the optical signal: micro-ring resonator, photo-detector, and transimpedance amplifier. The micro-ring resonator is used to couple a particular wavelength and remove it from the data waveguide. The coupled wavelength is fed into a photo-detector, which converts the optical signal into an electrical signal (albeit a very weak one)(optical to electrical conversion(O/E)). A transimpedance amplifier is used to amplify the received signal.

Detectors normally employ silicon-germanium or germanium-on-silicon technologies. Ge-on-Si detectors have shown responsivities and frequencies up to 1A/W and 40 GHz respectively [Lee et al. 2010] and have a delay of around 140ps [Koester et al. 2007]. Then, we need to integrate the detector with CMOS based post-amplifier circuits. The detectors' energy dissipation per bit is in the range of PicoJoules. It operates at 15Gb/s and has -7.4dBm sensitivity. Other choices of materials include ion-implanted silicon. The responsivity of this detector is 0.8A/W while using 1550nm signals. It can support bandwidths up to 10GHz [Geis et al. 2007]. Likewise, Miyamoto et al. [Miyamoto et al. 1998] have demonstrated a photodetector with a sensitivity of -27.8dBm at 40Gb/s.

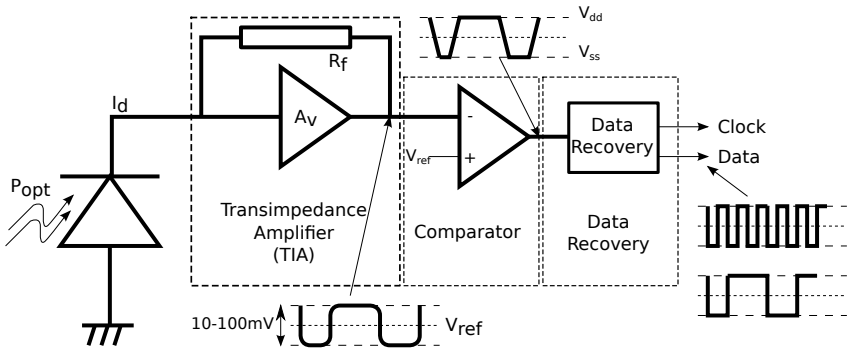

Fig. 13. Photo-detector circuit

In Figure 13, we show a typical photo-detector circuit. The transimpedance amplifier converts the photo-current of a few μA into a voltage of a few mV. The comparator is used to separate 0s and 1s, and the data recovery circuit is used to remove jitter from the signal.

3.4. Device Level Challenges

There are some key challenges that need to be addressed before the large scale adoption of photonic interconnects [Bogaerts et al. 2014] begins. For example, photonic devices are more prone to process variations than today's electrical components. Moreover, to connect the optical components together and ensure good signal integrity is an issue and a lot of design rules need to be created. EDA tools are relatively immature in this area. In this section, we will discuss the challenges in the design and fabrication of optical components that are necessary for optical communication. We have broadly classified these challenges into two broad categories: operational and fabrication challenges.

3.4.1. Operational Challenges.

Temperature Variations. In general, optical components are severely affected by temperature variation. The operation of optical components is highly dependent on the ambient temperature. Typically, chip temperature can vary by more than

30°C [Skadron et al. 2004]. This change in temperature can change the effective refractive index of the material. Specifically, the effective refractive index of a material is highly dependent on temperature and follows Equation 1, where n_0 is the refractive index at room temperature, $\triangle T$ is the change in temperature, and $\frac{\mathrm{d}n}{\mathrm{d}T}$ is the thermo-optic coefficient of the material.

$$n = n_0 + \frac{\mathrm{d}n}{\mathrm{d}T}(\triangle T) \tag{1}$$

This change in refractive index with temperature leads to changes in the resonant wavelengths of micro-ring resonators, emission wavelengths of lasers, and the operation of components such as MMI devices and directional couplers. For example, a change in temperature can cause a change in the resonant wavelength of ring resonators by 50-100 pm/K [Kim et al. 2010; Ye et al. 2014]. This drift in the resonant wavelength of micro-ring resonators can be mitigated using three methods. The simplest approach is to heat all the resonators to a pre-specified temperature, which is higher than the temperature at any point on the die. This approach known as *trimming* has been used in Corona [Vantrease et al. 2008], and is considered to be simple yet power consuming. The other approach is to change the refractive index of resonators by injecting current. However, as shown by Nitta et al. [Nitta et al. 2011] such an approach can quickly lead to thermal runaways. The injected current heats the resonator causing a red-shift, which further requires more current to introduce a blue-shift. If this process does not converge, then a thermal runaway is possible. The third approach is to use athermalized rings[Zhou et al. 2009; Timurdogan et al. 2014] that are less sensitive to variations in temperature. However, such devices are hard to fabricate.

Thus, Nitta et al. propose a solution based on trimming and current injection that uses a *Temperature Control Window*(TCW) and a sliding window based scheme. The TCW records the temperature range within which the rings need to be kept to prevent thermal runaway. Thus, a limited amount of current injection can be done(based on the current temperature and the TCW). To compute the changes in terms of current and trimming power, Nitta et al. simplify the problem by noting the fact that co-located rings have similar temperatures, and thus instead of trimming a single ring at a time, a group of co-located rings can be trimmed at the same time.

Akin to ring resonators, wavelength shifts in VCSEL lasers occur with change in temperature[Iga and Li 2003]. The emission wavelength of VCSELs changes as the temperature varies. The wavelength shift of a VCSEL laser with an operating range 800–1000nm is 70 pm per °C [Michalzik and Ebeling 2003; Saito et al. 1996]. Moreover, at higher temperatures the power efficiency of VCSELs also decreases significantly [Syrbu et al. 2008]. Ye et al. [Ye et al. 2011] have done a thorough analysis of the effect of temperature variation on modulation elements, switching elements and filter elements and showed that when the temperature reaches 85°C from 55°C, the power consumption of an optical NoC goes up to $5pJ/bit$ from $1.8pJ/bit$.

Charge Density Variation: The variation in the electronic charge density affects photonic devices. This variation changes the refractive index and the photon absorption capability of silicon [Soref and Bennett 1987]. The variation in the refractive index of the photonic device will disrupt the tuning of the device, resulting in either incorrect operation or the complete failure of the system. The variation in the free charge density is mostly due to accidental over or under doping; however, while carrying optical photons the charge density may change if the photons create additional electron-hole pairs. One of the common reasons for this is *Two Photon Absorption(TPA)* [Tsang et al. 2002]. A silicon atom can absorb two photons, and their combined energy will be trans-

ferred to the electrons. They can thus become free charge carriers. The refractive index will change because of the free charge, and the heat generated due to subsequent recombination.

Parasitics: Some amount of light invariably leaks out of optical components. This light can then travel to other optical components and disrupt their operation. The *parasitic light* includes the light signals generated due to back reflections, scattering of light at rough surfaces, and unwanted coupling between adjacent waveguides [Canciamilla et al. 2009; Bogaerts et al. 2014].

3.4.2. Fabrication Challenges.

Process Variation: . The term, *process variation*, refers to imperfections caused during the fabrication process. As a result, the dimensions of optical components deviate from their ideal specifications. *Wavelength drift*(for lasers or ring resonators) is one of the main problems that can happen due to process variation, resulting in a wavelength mismatch among various optical components. This may result in performance degradation, or in the worst case may result in unrecoverable data corruption. There are a lot of prior studies [Selvaraja et al. 2010; Chen et al. 2013; Chrostowski et al. 2014], which show that the process variation in silicon photonic interconnects is a serious issue. Xu et al. [Xu et al. 2012b] showed that an optical network without any process variation may lose more than 40% of its total bandwidth due to process variations. The variation in silicon thickness is considered as the major factor responsible for the non-uniformity in microring resonators. Zortman et al. [Zortman et al. 2010] reported that a variation greater than 10nm in the silicon thickness across a wafer induces a wavelength drift of ±9nm in microring resonators. Orcutt et al. [Orcutt et al. 2011] report a process variation induced wavelength drift of 4.79nm for ring resonators for different dies on the same wafer. Another recent study [Selvaraja et al. 2010] reveals that two micro-ring resonators placed 1.7mm apart showed a standard deviation of 0.55nm for their resonant wavelengths. In addition to silicon thickness, the other factors responsible for variation in optical components is variations in waveguide width, height and etch-depth [Krishnamoorthy et al. 2011].

One solution to take care of this issue is post-fabrication trimming using UV light or electron beams, which change the effective refractive index of optical components [Haeiwa et al. 2004; Schrauwen et al. 2008]. This process is slow, has limited efficacy, and increases the probability of ring resonators suffering from thermal runaway. The other solution is called *power trimming*. Here, the ring resonators are heated in order to compensate for the effects of process variations [Xu et al. 2012b; 2015]. A change in temperature can be used to alter the resonant wavelength.

Design and Integration: One of the most important problems in designing photonic interconnects is the placement and routing of waveguides, and other optical components [Condrat et al. 2013]. The optical waveguides are to be placed in such a way that we minimize the number of bends, and also choose the bends that are the most efficient in terms of power loss. Moreover, there should be sufficient distance between optical waveguides in order to reduce the optical coupling from one waveguide to another. In addition, at the interface of the optical device, the optical waveguide is required to match the port's geometry in order to decrease back-reflections, diffraction and scattering. Finally, since optical signals have a phase, the length of the interconnects should be adjusted in such a manner that whenever signals are combined, there is no signal loss due to a mismatch in the phase. The last problem is to reduce the number of waveguide crossings, because at every crossing some optical power is wasted (0.1-0.2dB [Koka et al. 2012]). One way to solve this is to use a 3D chip with optical through silicon vias (TSVs) across layers. However, in a high contrast material system, implementing efficient TSVs comes with some performance and integration penalties.

4. ARCHITECTURE

4.1. Summary

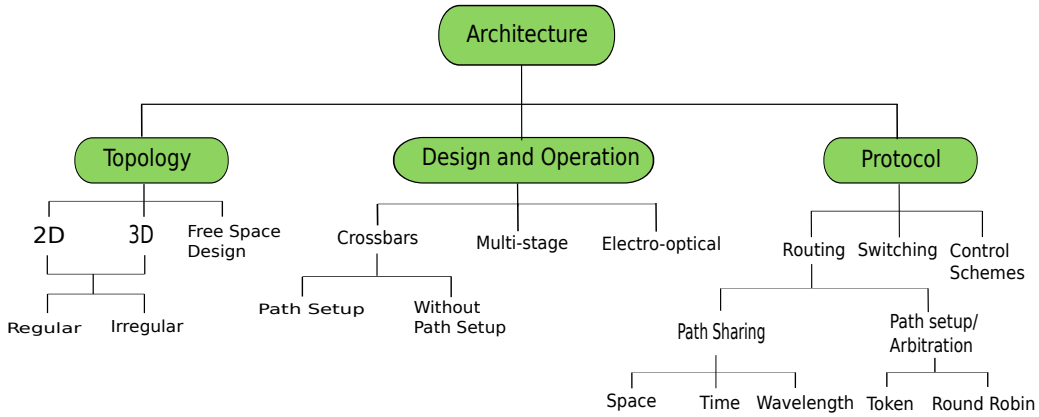

Fig. 14. Taxonomy of different architectures

In this section, we shall review popular on-chip photonic architectures. Figure 14 shows our proposed taxonomy of on-chip photonic architectures. Based on Figure 14, we divide this section into three major subsections: topologies (Section 4.2), design frameworks (Section 4.3) and protocols (Section 4.7).

4.2. Topology

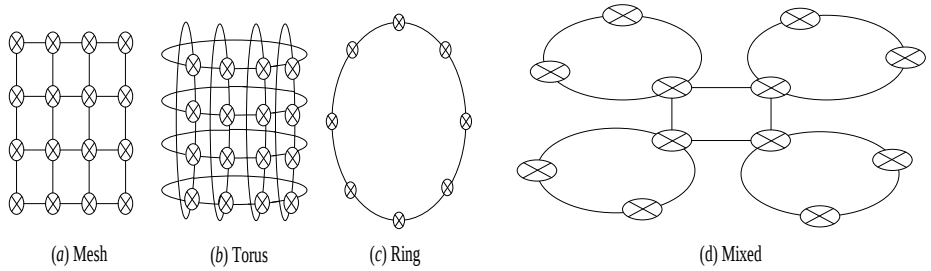

Fig. 15. Regular topologies

The job of an on-chip network is to deliver messages from one node to another in an efficient and reliable manner. The network should be laid down in such a way that every node has a logical connection to every other node in the network and there are reasonable bounds on the inter-node latency. The layout of a network is largely determined by its topology, which is defined as the physical layout of nodes on the chip. Regular topologies are the most commonly used topologies for on-chip networks. In a *regular* topology, all the nodes have roughly similar in-degrees and out-degrees. One of the simplest ways to classify different variants of extant regular topologies is based on the number of nodes in each dimension(k) and the number of dimensions(n), collectively referred to as k-ary n-cube topologies. An example of a regular topology is the

grid topology (k-ary 2-cube). The most commonly used grid topologies in on-chip photonic networks are the mesh and torus topologies [Bell et al. 2008; Vangal et al. 2008] because of their simplicity.

However, 2D mesh topologies have several disadvantages. One crucial disadvantage is that the message has to travel via many intermediate routers before reaching the destination leading to a higher latency. To rectify this problem, we can use high radix topologies such as the butterfly and clos topologies [Kim et al. 2007; Kao and Chao 2011]. Apart from mesh topologies, optical networks have been implemented with other regular topologies such as the crossbar [Tan et al. 2011], ring [Koohi et al. 2011] and torus [Ye et al. 2012] (refer to Figure 15(a),(b) and (c)).

4.2.1. 3D Networks. To optimize the performance of on chip networks, three dimensional integrated circuits (3D ICs) [Ye et al. 2009] are emerging as promising solutions because of various advantages such as a shorter inter-layer channel, higher bandwidth density and a reduced number of hops. There is a rich body of literature [Ye et al. 2009; Ramini et al. 2013; Ye et al. 2013] regarding 3-dimensional optical networks, which have multiple layers containing optical components connected with optical TSVs (through silicon vias).

A mixed interconnect with separate optical and electrical layers can be realized with 3D chip technology that uses TSVs [Ye et al. 2009] to communicate across the layers. Feero et al. [Feero and Pande 2009] have compared the performance of 3D and 2D based mesh and fat-tree topologies and found that the 3D implementation improves performance in both the cases. On the same lines, Ye et al. [Ye et al. 2013] proposed a 3D mesh based optical NoC in which all the optical routers are placed in a single layer in order to decrease the number of waveguide crossings and increase the scalability of the network.

Different types of regular topologies can be mixed to create hierarchical or hybrid topologies called irregular topologies. We can divide nodes on a chip into several clusters. Nodes inside each cluster can be connected with one type of topology and the clusters can be connected to each other using a different kind of topology. Figure 15(d) shows an irregular topology, which uses the ring and mesh topologies. Hierarchical topologies are *particularly advantageous* in optical networks because the entire network need not be powered on at the same time. A hierarchical topology allows us to power up only those parts of the network that need to be used.

4.2.2. Free-space Designs. Xue et al. [Xue et al. 2010] proposed a novel design with free-space optics to design optical interconnects for multicore processors. In this design each station has a set of lasers that beam their signals towards a plane that is parallel to the plane that contains the lasers. There is a separation between the planes. These signals subsequently are reflected by a set of small mirrors such that they reach the desired destination.

This is a fully distributed and scalable architecture, and is technically a $N \times N$ crossbar. Moreover, this design does not rely on any packet switching functionality, and allows direct communication between different nodes. However, packet collisions can occur due to the use of free-space signals. The only way to solve this issue is to add error detection and correction logic to the packets. We need to be able to detect collisions, and recover by either reconstructing the message using error correcting codes, or by retransmitting the message.

4.3. Design and Operation

The topology of a network (as we saw in Section 4.2) defines the interconnection of stations and waveguides. However, there are many ways of designing and operating an optical network with a given topology. It is sometimes the case that a given topology

constrains the architecture of an optical NoC and the methods of message transmission; however, there is a lot of flexibility in this regard, and we view both as different sub-areas, even though they are not strictly unrelated.

Let us divide this area into three broad category of designs: crossbar based designs, multi-stage designs, and opto-electrical (hybrid designs). A crossbar is a shared bus that can be used by optical stations to read and write messages. A very large fraction of related work is based on crossbars because they are very simple to design and operate, and also have natural support for multicast traffic. Multi-stage designs are more complicated, and are closer to traditional electrical networks where a path between nodes has to be setup via a network of intermediate nodes, and finally the last category – hybrid networks – is based on a combination of electrical and optical networks.

4.4. Crossbar Designs

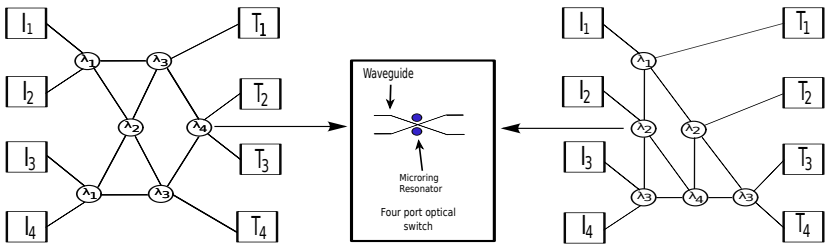

Fig. 16. Routers

Latency in on-chip networks is a key concern that needs attention. Latency highly affects the performance of the on-chip network. If networks are laid down in such a way that we have blocking links – a message might have to wait for other messages to pass – then in such cases the performance will degrade significantly.

One of the quintessential solutions for this problem is to provide non-blocking point-to-point links between the nodes so that messages need not wait for each other. As a result, latency decreases and performance increases. Keeping this in mind, researchers have proposed a variety of crossbars (a conceptual $N \times N$ link) for optical NoCs [Le Beux et al. 2011; Bianco et al. 2012; Ramini et al. 2013; Vantrease et al. 2008; Pan et al. 2009]. These crossbars rely on micro-ring resonators for routing and use wavelength division multiplexing for point-to-point connection through a shared waveguide. By providing contention-free routing, these crossbars have decreased the latency in on-chip networks. Optical crossbars are extremely popular as of today and most papers in nanophotonic networks use crossbars for at least a part of their network.

Most optical crossbars are implemented on a separate layer and use through silicon vias(TSVs) to connect the optical and electrical layers [Vantrease et al. 2008]. A critical disadvantage of using optical crossbars in on-chip networks is the associated optical loss due to the large number of ring resonators, waveguides, and waveguide crossings. Le Beux et al. [Le Beux et al. 2014] in a detailed study of the implementation of crossbars in on-chip optical networks, have provided insights into the tradeoffs between the area, latency, and complexity of crossbars. Given the importance of crossbars, many researchers have tried to decrease the number of micro-ring resonators and waveguide crossings in optical crossbars in order to reduce the optical losses.

The process of routing in optical crossbars is achieved by either setting up the path between the communicating nodes[Shacham et al. 2007; Cianchetti et al. 2009] and

then sending the message or by simply using dedicated links without path setup mechanisms[Kirman et al. 2006; Vantrease et al. 2008]. As a result two types of crossbar implementations are possible: with path setup and without path setup.

4.4.1. Crossbars with Path Setup. In such NoCs, the path between the source and destination is setup and then optical switches are used to change the direction of incoming signals. An optical switch can be made with a ring resonator, where depending on its state of resonance, it is possible to choose between two outputs for each input. These switches are configured before sending the message and after the path setup stage, messages between a sender-receiver pair always pass through a specific path. This path can be setup either optically [Shacham et al. 2007] (via a separate optical subnetwork) or electrically [Morris and Kodi 2010]. Most of the proposed on-chip networks that we discuss in this section use wavelength based routing mechanisms, where the optical signal is routed solely based on its wavelength at the intermediate switches. Matrix [Bianco et al. 2012], λ router [OConnor et al. 2008] and Snake [Ramini et al. 2013] are examples of routers that are used in such crossbars. Let us elaborate.

The Matrix router relies on a traditional matrix like structure. It has N stages, where each stage contains N optical switches. It thus uses $N \times N$ optical switches to provide full connectivity between N nodes. To decrease the number of optical switches, and consequently the number of ring resonators, the λ router was proposed by O'Connor et al. [OConnor et al. 2008]. It is a multi-stage design that tries to decrease the number of wavelengths and ring resonators. It uses wavelength based routing for signal propagation from the source to the destination. Like the Matrix router, it also consists of N stages of optical routers but each stage has fewer optical switches (see Figure 16(a)). The figure shows a 4×4 λ router connecting four nodes with each other. Based on the configuration of the switch, done at the time of path setup, it routes the incoming packet to the appropriate output terminal. Akin to the λ router, Snake is also a multi-stage crossbar with a difference only in the placement of ring resonators (see Figure 16(b)). Its design is considered to be more compact as compared to the Matrix and λ routers.

4.4.2. Crossbars without Path Setup. Most path setup based crossbar implementations do not scale well with an increase in the number of optical stations. Hence, researchers have proposed crossbar implementations without path setup. The tradeoff is that we need $O(N)$ times more waveguides for such networks. There are three different types of crossbars in this category: SWMR [Pan et al. 2009], MWSR [Vantrease et al. 2008], and MWMR [Pan et al. 2010].

(1) SWMR(Single Writer, Multiple Reader): In an SWMR bus, each station (writer) is connected to the rest of the stations (readers) via separate waveguides. If we have N optical stations, then this bus has $N \times (N-1)$ waveguides, where for each sender there are $N-1$ possible receivers. Furthermore, it is possible to send multiple bits in each cycle by using DWDM (wavelength multiplexing). Such buses naturally support multicast and broadcast based traffic. Each station sources some of the power on the bus using a beam splitter. If there are multiple stations in series, then setting the right split ratios of the beam splitters is a difficult problem. Peter et al. [Peter and Sarangi 2015] proposed a $O(N)$ time dynamic programming based algorithm to find the optimal split ratios such that the overall power loss is minimized. It can be implemented statically as well as dynamically.
(2) MWSR(Multiple Writer, Single Reader): An MWSR bus with N stations has N waveguides. There is a dedicated waveguide for each station. Now, for a given station it can only read from its dedicated waveguide. The rest of the stations can write to this waveguide. Since multiple stations cannot write to the same waveguide us-

ing the same set of wavelengths, we need to have an arbitration mechanism. The token channel and token slot algorithms proposed by Vantrease et al. [Vantrease et al. 2009] are some of the commonly used arbitration mechanisms.

(3) MWMR(Multiple Writer, Multiple Reader): Both SWMR and MWSR buses use dedicated channels for a source and destination respectively and this leads to an under utilization of link bandwidth and poor power efficiency due to over-provisioning of dedicated channels. Flexishare [Pan et al. 2010], a multiple-writer-multiple-reader(MWMR) crossbar, proposed by Pan et al. provides a mechanism to combine the SWMR and MWSR strategies in order to improve link utilization and reduce over-provisioning. It leads to a reduction in the number of channels at the cost of peak throughput. However, it requires arbitration at both the sender's side and the receiver's side.

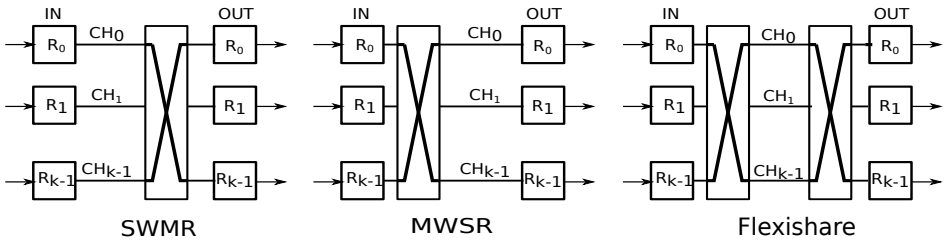

Fig. 17. Flexishare

4.5. Multi-stage Designs

We have two main goals while designing on-chip NoCs. The first is scalability in terms of power and performance, and the second is reducing complexity. Keeping such considerations in mind researchers have proposed multi-stage designs for on-chip optical networks, which are more scalable and efficient. Such hierarchical networks have tradeoffs between power, latency, and complexity.

One such design proposed by Le Beux et al. [Beux et al. 2010] tries to limit the number of optical switches and waveguide crossings in on-chip optical networks by dividing a large network into multiple smaller sub-networks. This design makes the network more scalable by limiting the number of switches but it uses extra waveguides and electrical signalling, which result in greater power consumption. A packet is first routed to an appropriate optical network using electrical signalling. It is then optically routed (wavelength routing) through the optical network and at the end electrical routing is used again to route the packet (from the optical station to the destination). Along these lines, Koka et al. [Koka et al. 2010] proposed a grid like multi-stage design. In this design electrical routers are used to switch the packets between nodes in rows and columns. However, it suffers from scalability issues. The "grids" used in this design cannot be extended to larger sizes in order to maintain power efficiency. A solution to this scalability issue was provided by the designs proposed by Morris et al.[Kodi and Morris 2009; Jr. and Kodi 2010]. These designs use shared photonic links to connect the different columns of a grid while the rows are fully connected with the help of crossbars.

4.6. Opto-Electric Designs

Standard features of modern electrical NoCs such as buffering, routing, and processing headers are very difficult to implement in optical networks. Hence, there is a school of thought that believes that it is wise to design hybrid networks. We can have small

electrically connected sub-networks at the lowest level, and then connect groups of cores or cache banks with an optical network. The simplest class of networks in this category separate the control and data planes. For example, Shacham et al. [Shacham et al. 2007] proposed a hybrid architecture for on-chip interconnects in which the arbitration of a photonic-shared medium is coordinated with the help of electrical interconnects. It combines a circuit-switched photonic network with a packet-switched electronic network. Similarly, Petracca et al [Petracca et al. 2008] proposed a hybrid network in which high bandwidth communication is made possible with the help of a photonic network and a concomitant electrical control network. These hybrid networks prove very efficient both in terms of performance and energy consumption as compared to their electrical counter parts [Hendry et al. 2009].

The next category of networks partition the network into two parts: electrical and optical. An early work by Kirman et al. [Kirman et al. 2006] uses a hierarchical opto-electric network to provide an efficient implementation of the Snoopy cache coherence protocol in optical networks. The design uses a loop shaped optical bus to transfer messages between clusters of cores. Inter-cluster communication happens through an optical interconnect and intra-cluster communication uses electrical interconnects. The main drawback of the architecture proposed by Kirman et al. is its lack of scalability because increasing the size of the network will lead to more electrical communication and that will overshadow the benefits gained due to optical communication. Corona[Vantrease et al. 2008] improves this design by assigning cores and cache banks to clusters. Intra-cluster communication is electrical, and inter-cluster communication is optical. Likewise, Firefly[Pan et al. 2009] is another example of a hybrid architecture in which nodes are also divided into clusters. Bahirat et al. [Bahirat and Pasricha 2009] also proposed a hybrid network with a ring shaped optical network for long distance communication and a mesh structured electrical network for short distance communication. On similar lines, HOME [Mo et al. 2010] uses a hybrid optical mesh based NoC, which utilizes optical and electrical interconnects in a hierarchical manner. Tan et al. [Tan et al. 2014] use high radix topologies and propose to combine a butterfly and fat-tree based network.

The last category of proposals relies on smartly choosing between the networks, or by reconfiguring them dynamically (turning on/off parts of the network, and varying the number of wavelengths). For example, to decrease the energy and latency while transmitting a message, Lego [Werner et al. 2017] chooses the best network among the two based on the distance between the source and the destination. In comparison, UC-PHOTON [Bahirat and Pasricha 2010] combines the 2D electrical mesh network with an optical ring based network in order to improve the packet latency and power consumption. It dynamically reconfigures the electrical and photonic networks in order to adapt to changing traffic patterns. On similar lines, the on-chip photonic network proposed by Artundo et al. [Artundo et al. 2009] reconfigures dynamically in order to handle the imbalance in traffic. It combines the electrical control network with a circuit switched optical network, which is reconfigured based on the communication pattern between a set of nodes. The authors provision for extra photonic links between pairs of nodes that are likely to communicate more.

4.7. Protocols: Routing, Switching, and Flow Control

After the on-chip photonic network is laid down, it is necessary to transport messages from a source to its destination in a reliable and efficient manner. We need switching, routing, and flow-control protocols. Switching refers to the process of choosing an output terminal for a given input terminal and data packet. Routing is defined as

the logic behind choosing a given output terminal given the eventual destination, and flow-control refers to the way we manage buffering and congestion in the network.

4.7.1. Switching Techniques. Switching techniques used in photonic on-chip networks can be categorized as either circuit switching or packet switching based techniques. In circuit switching, a dedicated link is first created between the source and the destination and after that the message transfer begins [Shacham et al. 2008]. The *reserved circuit* is kept intact till the end of the message transfer. This type of a connection oriented mechanism leads to insufficient utilization of communication channels. Alternatively, we can have a connectionless switching mechanism called packet switching in which no link is reserved for communication. Message transfer occurs dynamically between the source and the destination and the intermediate nodes take the routing decisions. One important advantage of switched networks as compared to point-to-point networks is that they are flexible and this leads to higher performance. However, they are limited due to higher optical power losses [Koka et al. 2012].

4.7.2. Routing in Optical Networks. Routing decisions made by intermediate routers in on-chip networks depend on the type of routing mechanism used. Routing mechanisms can be implemented either by logically splitting a shared path in terms of space, time, or wavelength, or by using arbitration mechanisms to elect a leader node, which can exclusively use the bus for a certain period of time. Hence, broadly speaking routing mechanisms in on-chip networks can be classified into two types – *path sharing* in terms of space, time or wavelength and *path setup* using arbitration mechanisms. Let us elaborate.

Point-to-Point. Most of the initial designs proposed for photonic on-chip networks use point-to-point links between the nodes and as a result there is a direct path between a source and a destination. Routing is per se simple. Beamer et al. [Beamer et al. 2009] used this method to connect two shared L2 caches and four memory controllers. Each L2 cache was shared by four cores. However, because of point-to-point links this design requires more waveguides.

Bus Based Broadcast. In this scheme, all the nodes in a network are connected by a broadcast bus such as SWMR and any element can broadcast (or multicast) a message using this broadcast bus. The message reaches the destination node, which removes the signal from the bus using ring resonators. Technically speaking for pure broadcast (multicast) based traffic, routing is not required. However, for additional power efficiency Pan et al. [Pan et al. 2009] suggested a mechanism called R-SWMR (reservation assisted SWMR). The main insight in this work is that most of the traffic in an optical NoC is predominantly unicast. Hence, we can keep all the receivers off by default. Whenever we need to transmit a message, the sender can send a 1-bit signal to the receiver using a separate waveguide called the reservation waveguide. The receiver can then turn itself on for the duration of the message transfer. This approach yields significant power savings and has become the default communication mechanism in various proposed SWMR buses [Peter et al. 2015; Peter et al. 2015].

Wavelength Based Routing. In wavelength based routing, the routing decisions by intermediate nodes are based solely on the wavelength of the carrier signal and do not depend on any information embedded inside the packet [Bergman et al. 2014]. In such routing mechanisms, the wavelength specific coupling property of micro-ring resonators is used to couple a specific wavelength from an input terminal to a predesignated output terminal. This type of routing has one important advantage, which is that it removes the O/E and E/O conversion overhead at the intermediate nodes and hence yields a more power efficient architecture. One such implementation of wave-

length based routing was proposed by Pan et al. [Pan et al. 2009] called Firefly. The proposed design uses independent wavelengths for various sender-receiver pairs in order to provide fully-optical communication. Kirman et al. [Kirman and Martínez 2010] shows that it is possible to significantly reuse wavelengths for paths that are disjoint. A criticism of such works is that we typically have a narrow bandwidth (1-4 bits) channel between source-destination pairs. This significantly reduces the gains of optical NoCs. Since the routing mechanism is pre-decided, it is hard to allocate more bandwidth, even if other parts of the network are idle. Such kind of routing is also known as *oblivious routing*, because the path between a sender and receiver is independent of the nature of traffic in the network. However, Chan et al. [Chan and Bergman 2012] propose a mechanism to increase the performance in such networks by interleaving some extra wavelengths between the resonating wavelengths of a microring. These extra wavelengths can be used to provide additional bandwidth.

Routing using Arbitration. Most of the on-chip optical network communication strategies rely on shared resources. If multiple nodes want to access a shared resource that is not pre-emptible then an arbitration mechanism may be required for granting exclusive access. An example of such a shared resource is an MWSR bus.

4.7.3. Token based Arbitration. Token based arbitration is the most popular technique for arbitration. It guarantees that no two nodes are accessing the same resource and also provides freedom from starvation. A separate waveguide is used in which an optical signal acts as a token. Presence of light in this waveguide means that the token is available. Whenever a node wants exclusive access to a resource, it grabs the token by extracting light from the arbitration waveguide using a micro-ring resonator and after sending data it releases the token by injecting light into the arbitration waveguide. Even though the broad idea is simple, there are issues with regards to fairness and starvation that need to be addressed. Let us look at some of the recently proposed token based mechanisms.

— **Token Channel** [Vantrease et al. 2008]: A dedicated circular waveguide known as an arbitration waveguide passes through all the stations in a network. It carries tokens, where each token is represented as a single cycle pulse at a given(unique) wavelength. Before a station can send data on a waveguide, it needs to grab its corresponding token from the arbitration waveguide. This can be done by tuning its ring resonators such that the light pulse corresponding to the token is removed from the waveguide. Subsequently, when the station is done with transmitting the message on the data waveguide, it can *release* the token by transmitting the single cycle pulse on the arbitration waveguide. Either some other station will absorb the light (token), or the token will become unused(free). There is a dedicated home node that keeps track of unused tokens, and regularly transmits pulses corresponding to them. This scheme guarantees mutual exclusion; however, it has fairness issues.
— **Token Slot** [Vantrease et al. 2009]: To overcome the limitations of the token channel scheme, the token slot arbitration mechanism was proposed. This arbitration mechanism divides the communication channel into back-to-back fixed size slots and circulates tokens for each slot (similar to time division multiplexing). Whenever a node wants to send data in some slot it waits for the token for that slot and then sends data. The destination receives the data and then re-injects the token into the arbitration waveguide for that time slot. Since the destination does the re-injection, the token will be available as soon as the data transmission is completed in that time slot. Moreover the data waveguides may carry the data corresponding to different sources simultaneously at different points on the waveguide. We thus have efficient channel sharing in this technique. Finally, note that this mechanism

also results in a more power efficient NoC as compared to the token channel scheme because of the high utilization of data waveguides.

— **Two pass token stream** [Pan et al. 2010]: The daisy chain like design in the token channel and token slot protocols creates fairness issues. The two pass token stream based protocol guarantees greater fairness. In this scheme a stream of tokens is sent on an arbitration waveguide. The arbitration waveguide makes two passes around all the stations. For N stations, we have N waveguides, and we pass N tokens (1-bit signals at different wavelengths). There is a one-to-one mapping between tokens and waveguides. Any station that wants to send data can grab its corresponding token and send data on its dedicated data waveguide. It is possible that some tokens are not grabbed in the first pass. They will travel through all the stations in the second pass. In the second pass, these tokens can be grabbed by any station, and then the winning station can exclusively use the waveguide corresponding to the token. This scheme combines the benefits of a dedicated token scheme and the daisy chain scheme to provide a starvation free arbitration mechanism. However this mechanism is still not completely fair because the nodes closer to the home node (token injector) have higher priority in the second pass.

— **Feather Weight** [Pan et al. 2011]: Pan et al. proposed an arbitration mechanism that not only provides mutual exclusion and freedom from starvation, but also provides guaranteed fairness. The proposed mechanism works by providing a quota (maximum number of tokens) to a station. The station after consuming its quota cannot grab extra tokens in the current epoch but should rather wait for the next epoch. At the end of every epoch the stations send their runtime statistics to a QoS (quality-of-service) controller, which then calculates the quotas for different stations in the next epoch. This feedback mechanism helps us prove some bounds on the difference in the perceived fairness between two stations. Moreover, this design also leads to a power efficient NoC because the tokens are allotted depending upon actual usage. The main drawback of this scheme is that at the end of every epoch some cycles are used to collect statistics and distribute tokens to the stations. During these cycles, all the stations have to be idle and hence this may result in a decrease in performance.

4.7.4. Flow Control Schemes. A sender can send data to any node in a network; however, the receiver may not be able to read the data because it may have run out of buffer space. To ensure that this does not happen very frequently, we need *flow control* mechanisms.

The most commonly used flow control mechanism [Pan et al. 2010] is based on credits. Consider a system with MWSR buses. Let us add an additional arbitration waveguide where every reader node circulates a token with a certain number of credits. The number of credits is equal to the number of messages the reader can receive. Whenever a writer needs to send data to a reader, it needs to first grab the credits token corresponding to the reader, decrement the credits if available and then send the data. The token is then re-circulated in the arbitration waveguide. If a node grabs a token with no credits left, it will not send any data. It will rather forward the token and wait to get the token once again with hopefully non-zero credits. Whenever the token reaches the reader, it refills it with the number of available buffers. This scheme can have fairness issues. They were solved in a later paper by the same authors [Pan et al. 2011].

5. POWER REDUCTION

5.1. Overview

Power consumption is considered to be one of the largest bottlenecks in the adoption of optical technology on a silicon chip. Many research proposals [Zhou and Kodi 2013; Pan et al. 2010; Mohamed et al. 2014; Bashir and Sarangi 2017; Peter et al. 2017b] have taken into account the fact that power dissipation is an important problem in on-chip optical networks. In specific, static power consumption is the dominant form of power consumption. Static power consumption due to off-chip lasers and the thermal tuning of micro-ring resonators dominates the overall power budget of photonic NoCs. Pan et al. [Pan et al. 2010] have shown that in a radix-32 crossbar, 74% of the optical power is attributed to the laser and tuning power (i.e., static power). The problem of power consumption in optical networks is compounded by network insertion losses (losses in waveguides, and couplers), and the use of separate messages for arbitration and reconfiguration. In this section we describe various sources of power consumption in photonic on-chip networks and briefly discuss various proposals for reducing power consumption.

Figure 18 shows a taxonomy of proposals in this area. In Section 5.2 we discuss static power consumption in on-chip photonic networks and in Section 5.3 we describe the problem of dynamic power consumption. In each section we also discuss the solutions to reduce power consumption and the limitations thereof.

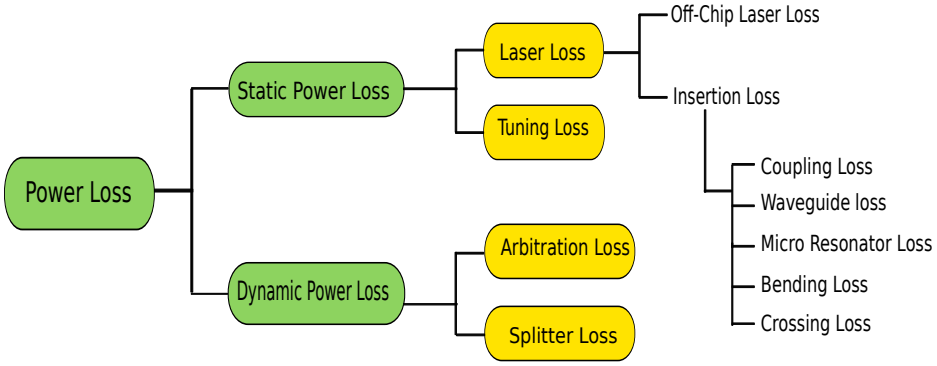

Fig. 18. Sources of power loss in optical networks

5.2. Static Power Consumption

The power that is wasted in optical networks and is not used for message transfer is called static power consumption.

5.2.1. Laser Power Loss.

a) Network Insertion Loss: The network insertion loss includes the optical loss, which occurs due to the coupling of light between waveguides and in the propagation of light through bends, resonators, and waveguide crossings. When an optical signal propagates through a network, it encounters various optical components, which results in the attenuation of the optical signal. The reason for this is that there is some leakage of optical power while the signal travels through waveguides($\approx 0.5dB/cm$), resonators in the off state($0.005dB$), resonators in the on state($0.5dB$), crossings($0.15dB$), and bends($0.005dB/90°$) [Werner et al. 2015; Chan et al. 2010]. In addition, when the laser source is outside the chip, we have to couple the optical power into the chip. This is a lossy process and results in a large amount of optical power loss via the tapers (see Section 3.2.1). An immediate solution is to have more efficient optical devices such as

a power efficient coupler [Humphrey 1994]; however, increasing the power efficiency of optical components has its limits, and often a solution at the architectural level is required.

Any solution at the architectural level needs to have smaller (straighter) waveguides, minimize crossings and bends, and avoid connecting many components (even if they are passive) in series. However, most of the popular proposals [Pan et al. 2009; Vantrease et al. 2008; Vantrease et al. 2009] connect all the tiles in the chip by having very long waveguides that often make multiple passes around the stations. Due to these long waveguides there is a significant amount of power loss. For example, the total waveguide length in a 400 mm^2 die is estimated to be 9.5 cm and 5.5 cm for the Firefly and Clos networks respectively. This will lead to 4.75 dB and 2.75 dB loss in optical power, assuming a waveguide loss of 0.5 dB/cm (this figure can be more also). Many papers have used values of 1 dB/cm as well. The LumiNOC architecture proposed by Li et al. [Li et al. 2015] proposes solutions to most of these problems. It is based on decreasing the length of the waveguides in order to reduce the waveguide losses. The authors have proposed to divide a large NoC into smaller subnets in order to limit the length of the waveguides. The other solution to decrease the insertion loss is to decrease the number of bends by using a serpentine shaped waveguide [Vantrease et al. 2008] and decrease the waveguide crossings by stacking optical layers on top of each other(3D stacking [Morris et al. 2012; Ye et al. 2013]).

b) Off-chip Laser Loss : An off-chip laser is the most commonly used light source in on-chip optical networks. In principle, the laser should be active all the time and provide power to all the nodes. Whenever a node wants to send data, it sources some part of the power provided by the laser source, modulates the signal, and sends it to the destination.

As we had discussed in Section 2.4 optical networks are naturally constrained by the fact that photons cannot be stored. Hence, it is necessary to transmit photons (light) all the time, and the flow of light (or the lack of it) determines the logic levels of the transmitted data. However, keeping the lasers on all the time consumes a lot of power, and is definitely not desirable, because optical stations are not transmitting all the time.

Hence, most papers today try to solve this problem. A common approach is to divide time into epochs (fixed intervals of time). The power that the lasers deliver is fixed in an epoch. This power is distributed among the stations using a set of waveguides known as *power waveguides*. Moreover, in a given epoch, we predict the power required for a subsequent epoch(see [Peter et al. 2015; Zhou and Kodi 2013]). There are several ways of doing this. In the Probe [Zhou and Kodi 2013] project, the authors make a prediction based on the link and buffer utilization. In comparison, ColdBus [Peter et al. 2015] adopts a different approach. In ColdBus, the authors make a prediction based on the predicted number of L1 cache misses, where the program counter is used for prediction. After the prediction, a message is sent to configure the lasers. This can take varying amounts of time depending on the type of the technology used. In Probe it takes 100 CPU cycles (at 2 GHz) for a 1000 cycle wide reconfiguration window, whereas in ColdBus it is much faster because the authors use fast single cycle splitters [Peter et al. 2016], and DML lasers that can be modulated within a several hundred picoseconds. Likewise, the authors of EcoLaser [Demir and Hardavellas 2014] also propose to turn the lasers off, when we observe reduced activity. The ESPN architecture proposed by Li et al. [Li and Li 2013] uses various independent lasers for different portions of the network. Each laser is turned on and off based on the activity in its sub-network.

There can be mispredictions in the sense that we can either under or overestimate the power required. If there is an underestimation, then there are several options.

Works such as Probe propose to delay message transmission till the next epoch. ColdBus uses an additional waveguide called an *extra waveguide* that delivers contingency power. This is shared among the stations, and it is necessary to arbitrate for the power using a token based arbitration scheme.

The other solution to decrease this source of power loss is to increase the utilization of the optical power by allowing stations to share the optical power. Flexishare [Pan et al. 2010] proposes a variant of the MWMR topology in which the stations are allowed to share the optical channels and consequently the laser power. This decreases the number of optical channels and increases the power utilization. Likewise, Zulfiqar et al. [Zulfiqar et al. 2013] proposed a wavelength stealing method that uses opportunistic channel sharing to improve the bandwidth and reduce the power consumption. Each node is assigned a channel. A channel, which is unused by its node for the time being, can be used by other stations to get an increased bandwidth.

5.2.2. Tuning Loss. Given the thermal sensitivity of ring resonators, it is necessary to ensure that they always operate at a pre-specified temperature. The standard approach is to use micro-heaters such that the temperature of the rings can be maintained at a certain level. These micro-heaters however consume a fair amount of power, and as per estimates the total ring heating power (also known as the *trimming* power) can be as high as 20-40% [Vantrease et al. 2008; Joshi et al. 2009; Pan et al. 2010] of the total optical power. A standard value of 26μWatts per ring is typically used as the ring heating power [Pan et al. 2009].

One possible solution to decrease this is to reduce the number of resonators [Le Beux et al. 2011]. Two projects, SUOR [Wu et al. 2014] and ORNoC [Le Beux et al. 2011], propose to partition the data waveguides into segments and allow multiple transactions (in both directions) at a time. This allows us to use a lower number of data waveguides, and we can thus reduce the number or ring resonators. ORNoC statically assigns wavelengths and sections of waveguides to stations, whereas SUOR uses a method based on arbitration. Likewise, there are many other proposals such as RPNoC [Wang et al. 2015], QuT [Hamedani et al. 2014] and AMON [Werner et al. 2015], which try to reduce the number of ring resonators. Both RPNoC and QuT are ring based topologies in which a wavelength based routing method and a novel wavelength assignment mechanism are used to reduce the number of required wavelengths, thereby reducing the number of ring resonators. On similar lines, AMON is a mesh based network, which divides a network into smaller sub-meshes and allows the wavelengths to be reused across different sub meshes, thereby reducing the number of wavelengths and the number of ring resonators. A channel borrowing design proposed by Xu et al. [Xu et al. 2012a] describes how two nodes can share a waveguide by borrowing channels from each other.

5.3. Dynamic Power Loss

Dynamic power consumption refers to the power consumed in sending messages between stations in on-chip optical networks. The sources of dynamic power consumptions are as follows. The first source is the power consumed in the transmission and photo-detection circuitry. The transmitter performs E/O conversion, and the photodetector at the receiver converts the optical signal to electrical current. In addition, the receiver has TIA amplifiers to convert the small current pulse generated by the photodetector to a signal at the CPU's logic levels. The energy consumed due to O/E and E/O conversion is estimated to be around 2.6pJ/bit at an 80nm design [Kromer et al. 2005].

The second source of dynamic power consumption is the power required to perform arbitration and get exclusive access to the waveguides. This is dependent on the type of arbitration used. Let us now look at the third source of power loss, which is by far

the most dominant. If we are transmitting optical power, or a message to a set of optical stations, it often needs to pass through a set of splitters arranged in series. These splitters divert a fixed proportion of the power to their connected optical stations. However, the process of splitting a signal is not ideal; some part of the signal is dissipated as heat.

5.3.1. Splitter Loss. The theoretical problem is as follows. Consider a sender, and n (≥ 1) receivers, where each receiver receives its power via a beam splitter. We need to transmit a message while consuming the least possible amount of power.

Let us first consider a system with splitters connected in series. Some works such as ATAC [Kurian et al. 2010] proposed a methodology where the splitters have split ratios as follows: $1/n$, $1/(n-1) \ldots 1/2$. This is however not optimal when we have a non-zero loss in the splitters. This problem was solved by Peter et al. [Peter and Sarangi 2015]. For each category of splitters, they synthesized 200 separate designs and plotted the split ratio and the power loss. The envelope of this curve corresponds to the design that has the lowest power loss for a given split ratio. Subsequently, they proposed a dynamic programming algorithm that has a linear time complexity. The algorithm uses lookup tables, and computes the optimal solution for a system with n nodes by first computing the optimal solution for a system with $n-1$ nodes. The SWMR bus proposed using this algorithm is 87% more power efficient than the solution proposed in ATAC. This problem was also open for trees. There was a solution proposed by Binzhang et al. [Fu et al. 2010], which took exponential time. Peter et al. [Peter and Sarangi 2015] further improved this algorithm using a variant of their dynamic programming technique that they had proposed for a chain of nodes. Their algorithm is optimal for both chains and trees. A hardware implementation for trees takes 32 cycles for 64 stations with a 2.5 GHz clock. This algorithm can be coupled with a system that has a fast tunable splitter that can change its split ratio in a fraction of a clock cycle. Peter et al. proposed such a splitter using ring resonators based on partial resonance in [Peter et al. 2016].

6. APPLICATIONS

6.1. Overview

Due to low latency and high bandwidth, optical interconnects can be used for different kinds of applications. For example, in many applications we need to broadcast the message to all the nodes very quickly and for such applications we can use an on-chip optical broadcast network. Snoopy cache coherence is the quintessential example in this category. However, there are other applications such as the implementation of barriers, arbitration (already discussed in Section 4.7.3), and NUCA protocols in L2 caches. Let us elaborate.

6.2. Snoopy Cache Coherence

The snoopy coherence protocol uses a broadcast bus on which the nodes snoop for messages with addresses that they might have cached. In electrical networks, the snoopy cache coherence protocol is not scalable. As a result, the directory protocol is preferable. However, because of the inherent advantages of optical networks namely low latency, high bandwidth, and support for multicast operations, implementing this protocol is a feasible option for much larger systems of cores. Kirman et al. [Kirman et al. 2006] describe one such solution. Here, the nodes snoop on messages sent on a shared optical interconnect.

The nodes send their requests using different wavelengths. All the other nodes snoop on the requests and arbitrate among these concurrent requests. All the nodes arrive at the same final decision regarding the request that should be serviced (for different requests to the same line). The selected requests are processed in all the caches

simultaneously, and the remaining requests are retried later. The caches send their responses to all the other nodes through an optical snoop response bus and the data to be sent is sent through a data waveguide. On similar lines, Xu et al. [Xu et al. 2011] propose an implementation of a snoopy cache coherence protocol in large NoCs using an optical network.

6.3. Barriers

Barriers are used to synchronize multiple threads. One of the earliest proposals in this area was by Binkert et al. [Binkert et al. 2009]. Their approach is simple, and mainly consists of broadcasting the barrier release signal on the optical bus. However, they do not take care of context switches and the presence of simultaneous barrier operations. Chandran et al. [Chandran et al. 2016] have proposed a far more generic barrier implementation that takes into account thread migrations and context switches. It is also distributed in nature, and is thus more scalable than implementations with centralized structures.

6.4. LLC Access Protocol

Some of the best electrical last level cache (LLC) access protocols divide the set of cache banks into sets, and allow a line to migrate among the banks in a set. In steady state, the frequently accessed lines are found to be closer to the requesting cores. Due to topological constraints, these bank sets are often linear rows or columns. Peter et al. [Peter et al. 2017a] proposed a protocol for accessing large LLCs using optical networks. They observed that given the speed and bandwidth of optical networks, we are not constrained by the topology any more. We can have arbitrarily shaped sets (called overlays) that contain banks from all over the chip. Having such flexible overlays allows us to very efficiently manage the accesses in an LLC, decrease the miss rate significantly, and then realize significant gains in performance.

6.5. Virtual Chip or Macrochip

Using a large number of cores on a chip has some inherent problems such as the resultant large area, low yield, high power consumption, and large off-chip bandwidth requirements. These constraints have become a bottleneck in the scalability of single and dual chip based server design. One solution is to have smaller chips (chiplets) and then create a single virtual chip. But the delay in inter-chiplet communication can greatly reduce the performance of the entire system. However, by using optical communication to connect these chiplets, we can potentially lower the delay in message transfers. Krishnamoorthy et al. [Krishnamoorthy et al. 2009] have presented some early ideas with regards to the architecture of a macrochip and the optical component requirements for such a chip. Likewise, Demir et al. [Demir et al. 2014] proposed the design of a large virtual chip by using smaller chiplets in order to make the chip substantially scalable. This design uses optical fibers to connect chiplets with each other and has 1.8-2.2X more performance than an equivalent single chip with optical interconnects.

7. FUTURE PROSPECTS AND CONCLUSION

In this paper we presented a comprehensive survey of on-chip photonic networks. We started out with the different layers in on-chip optical NoCs, and then proceeded to describe the main components in an optical communication system: different topologies, routing protocols, power management strategies, and applications.

Most of the basic technologies for designing basic optical networks are well established, and robust prototypes of most devices have been fabricated in industry. Some system level challenges however remain. Integrating hundreds, or possibly thousands

of optical components on a chip at an industrial scale remains to be done. Even though other assorted challenges such as power management, trimming, and handling parameter variation have been taken care of to some extent, still we are several years away from realizing a server scale chip that can fully leverage on-chip optical networks. These will be exciting times for researchers in both academia and industry.

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