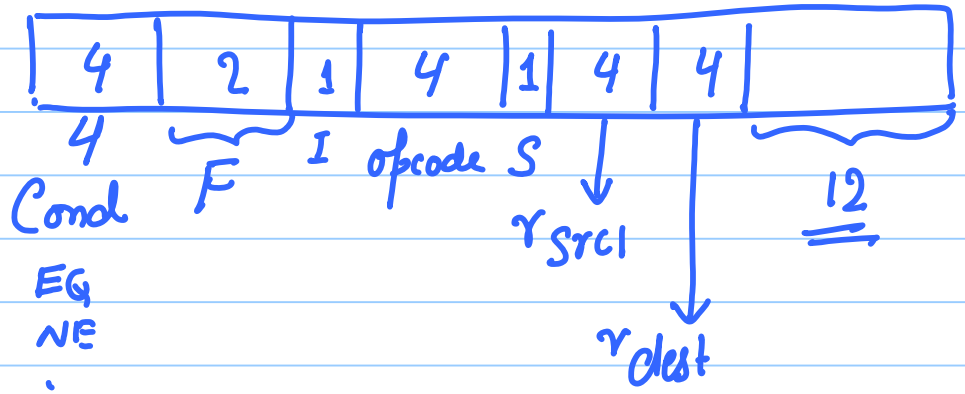
Note Title 07-08-2012

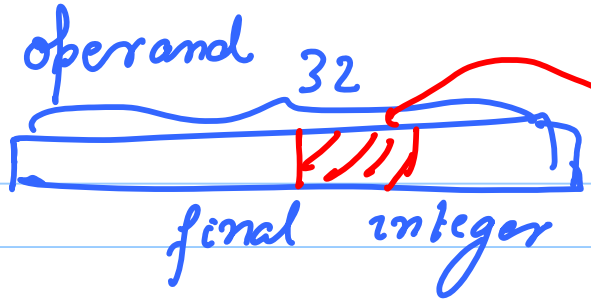
August 7th

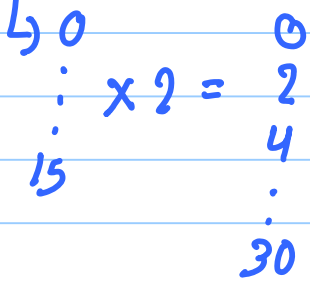
Instruction format



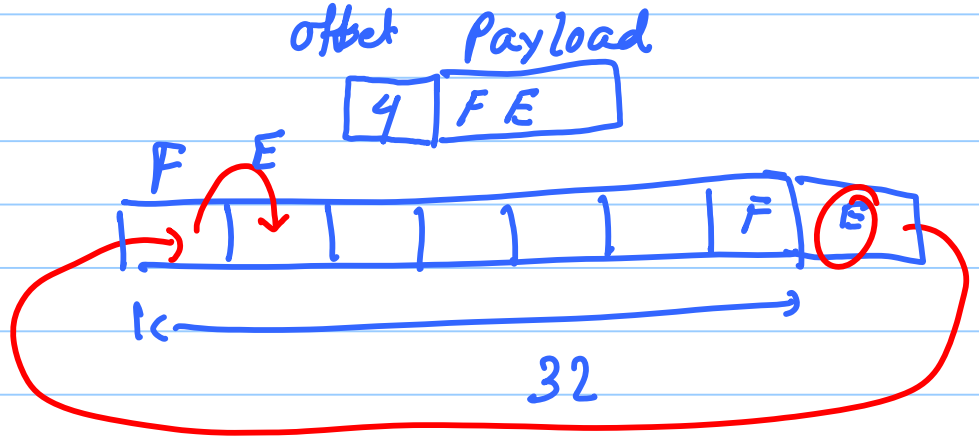
12-bits

1) Immediate operand



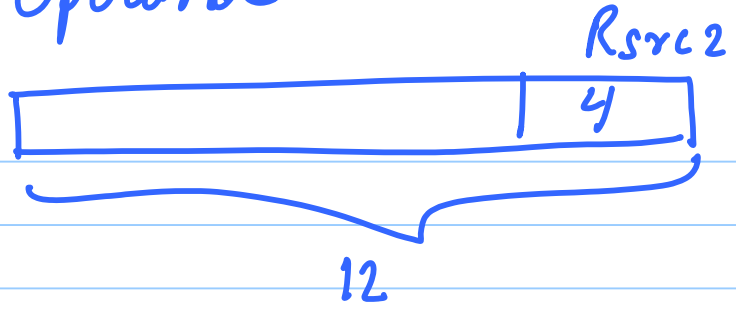


Number : Payload ROR (2×offset)



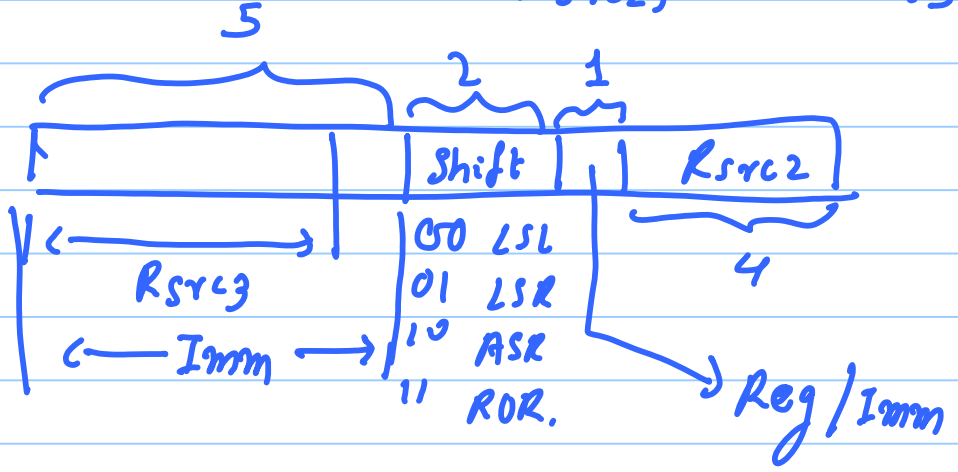
offset × 2 = 8

2) Register Operand



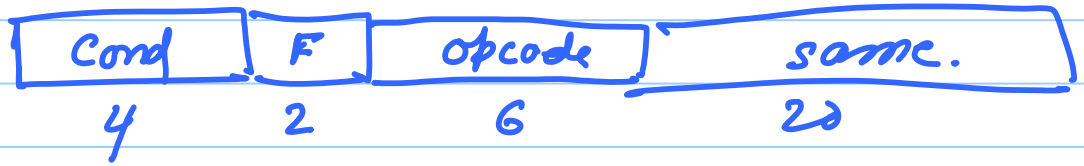
3) Shifted register

Rsrc2 LSL Imm (Imm)
Rsrc2, LSL Rsrc3 (reg)



```
ADD   R3, R2, R1, LSL R0
ADD   R3, R2, R1, ROR #29
```

Load/Store.



Usage

```
LDREQ   R2, [R4, R3, LSL R0]
STRNE   R2, [R4, R3, LSR #9]
```

for(i=0; i<100; i++)

A[i]=0;

STR R0, [R5, R1, LSL #2]

X ADD R1, R1, #1

pre-indexed

STR R0, [R5, #4]!

mem[R5+4]=R0

mem[R5]=R0

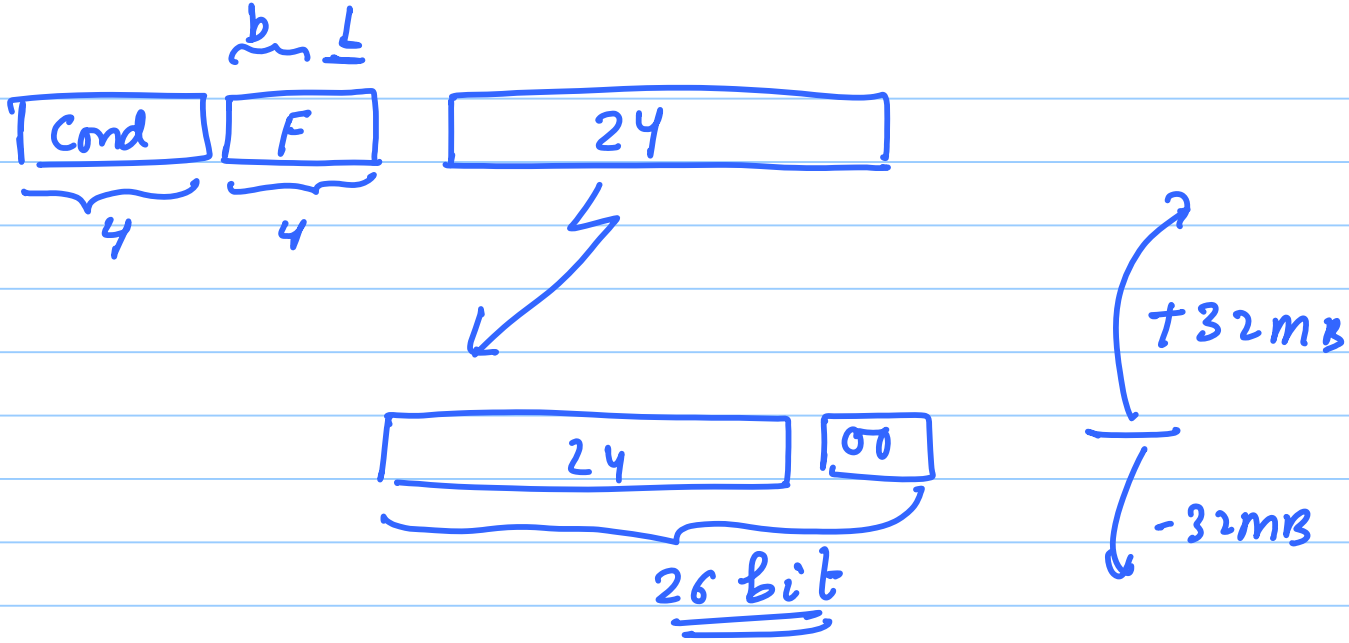
Or

post-indexed

STR R0, [R5], #4

R5 = R5 + 4 (pre/post)

Branches



1 B 1000

2

3

new PC = oldPC + 1000 + 8

MOV R0, PC