Oct. 17

Note Title 17-10-2012

Opcode
(ADD / ld / st / Br)

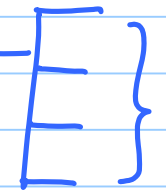
TRACE
10 million +

IF stage - Br pred

↙

Correct

Cache - II

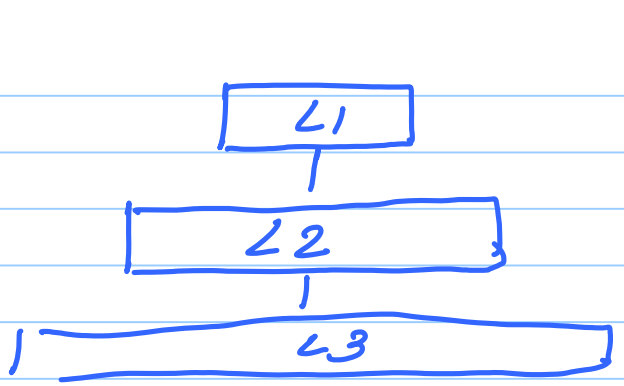
Set.  Cache Lines.

Extra state with cache line:

Valid bit (0/1)

Modified bit (0/1)

Cache Read

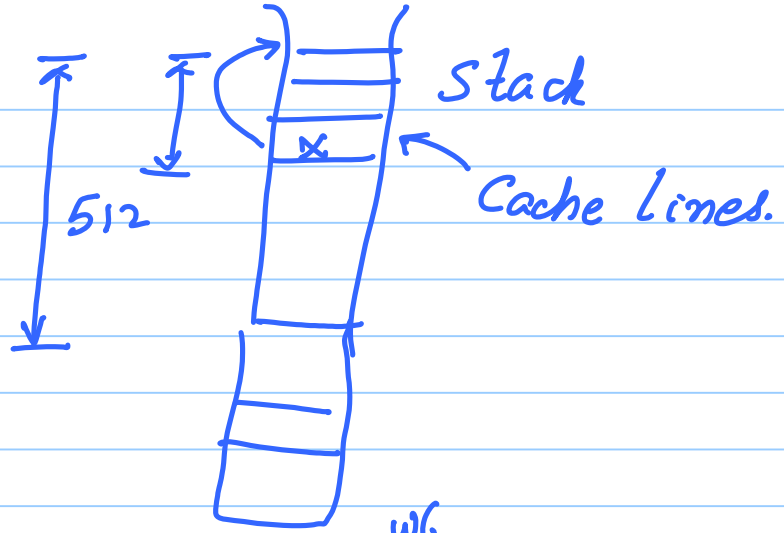


set-

Replacement Policy: Evict a line from the set.

LRU → timestamp

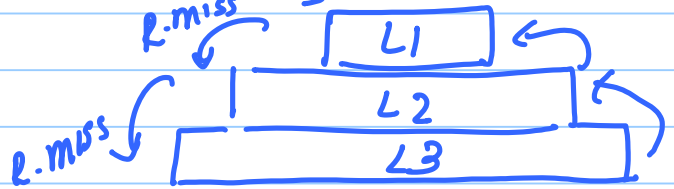
FIFO → oldest one is out.



$$M.R \propto \left(\frac{1}{\sqrt{size}}\right)$$

Set.

Writes:

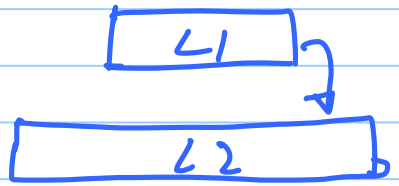


Modified bit:

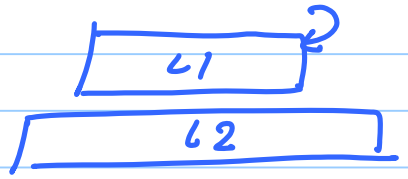
Whenever you write a blk
→ set $m \to 1$

Two policies

Write Through (WT)



Write Back (WB)



Eviction:

(WT) → Just Evict

WB → Write to lower level if (m == 1)

Base CPI = 1.5

% of mem insts: 1/3

		Penalty
L1 Miss Rate:	20%	10
L2 (LOCAL) Miss Rate:	40%	100

L2 Miss → LOCAL, GLOBAL

LOCAL: $\frac{\#\ \text{MISSES}}{\#\ \text{ACCESSES}}$

GLOBAL: $\frac{\#\ \text{MISSES}}{\#\ \text{MEM. INSTS}}$

$$CPI_{new} = 1.5 + \frac{1}{3}\left(0.2 \times 10 + 0.2 \times 0.4 \times 100\right)$$

Misses —
- Compulsory — (Prefetching) — FIX
- Capacity — (Size ↑)
- Conflict — (Assoc. ↑)

Multi - Process

Virtual Memory

- Isolation
- Large addr. space