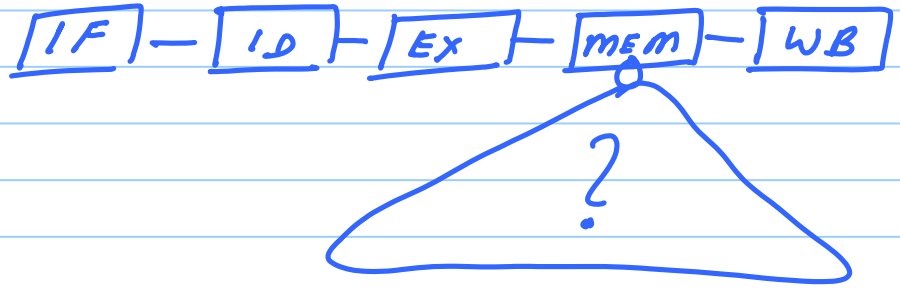
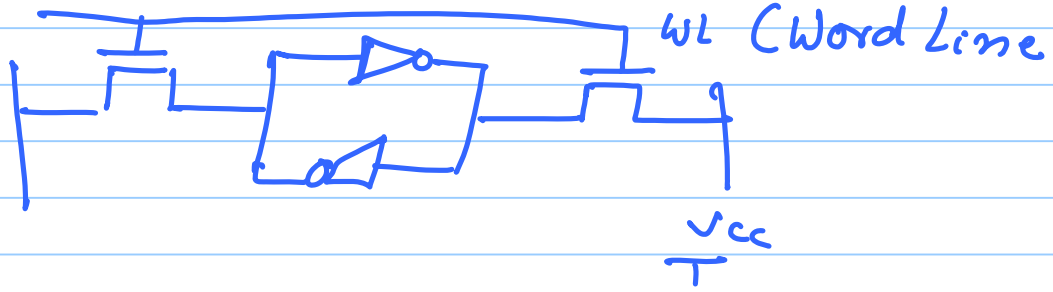
The Memory System

Note Title 10-10-2012

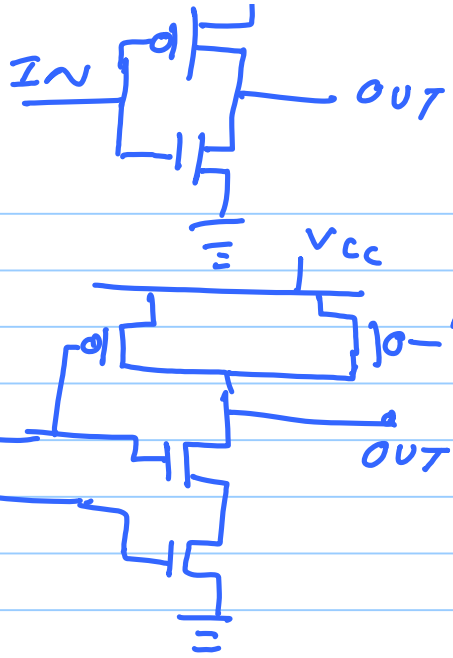


Elements of a memory system:

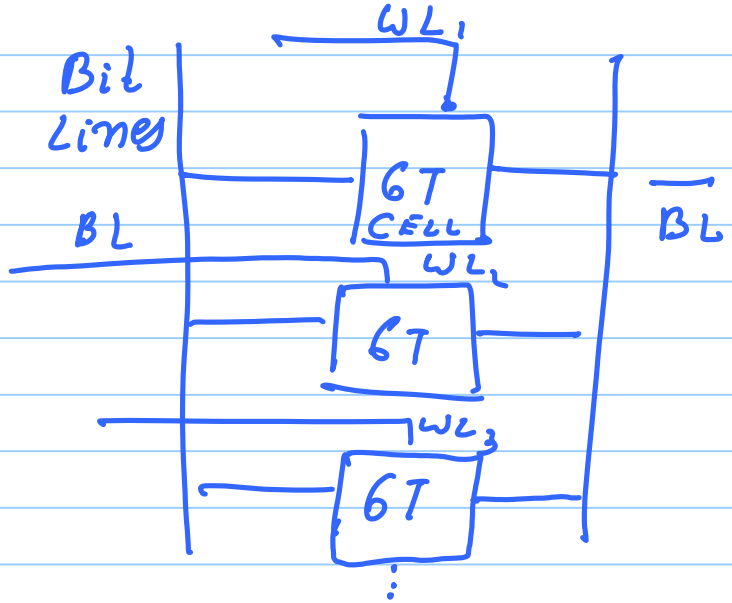
SRAM cell (Static RAM cell)

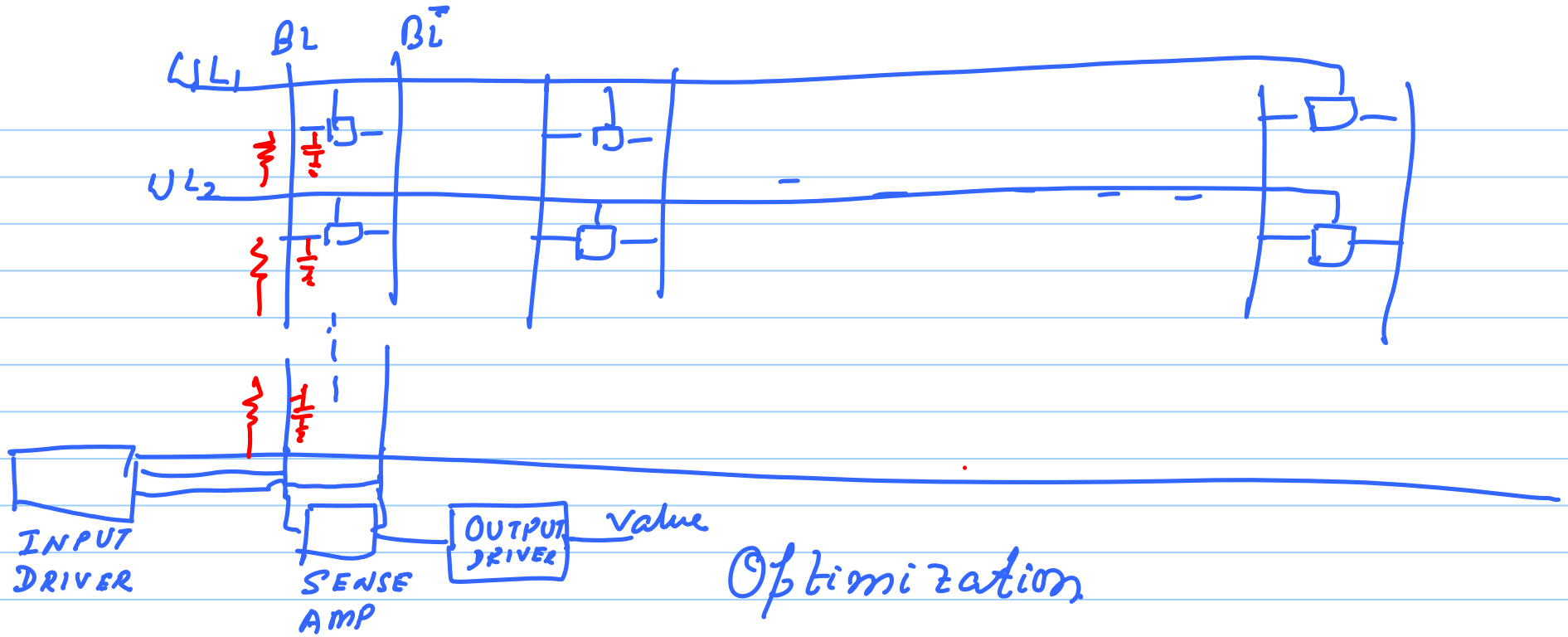



INVERTER


IN
OUT
Vcc
B
A
OUT
B


A
B
NAND


WL1
Bit Line
6T CELL
BL
BL
WL2
6T
WL3
6T



Optimization

1) Pre-charge BL and $\overline{BL}$ to 0.5 V

2) Monitor $\Delta = (V_{BL} - V_{\overline{BL}})$

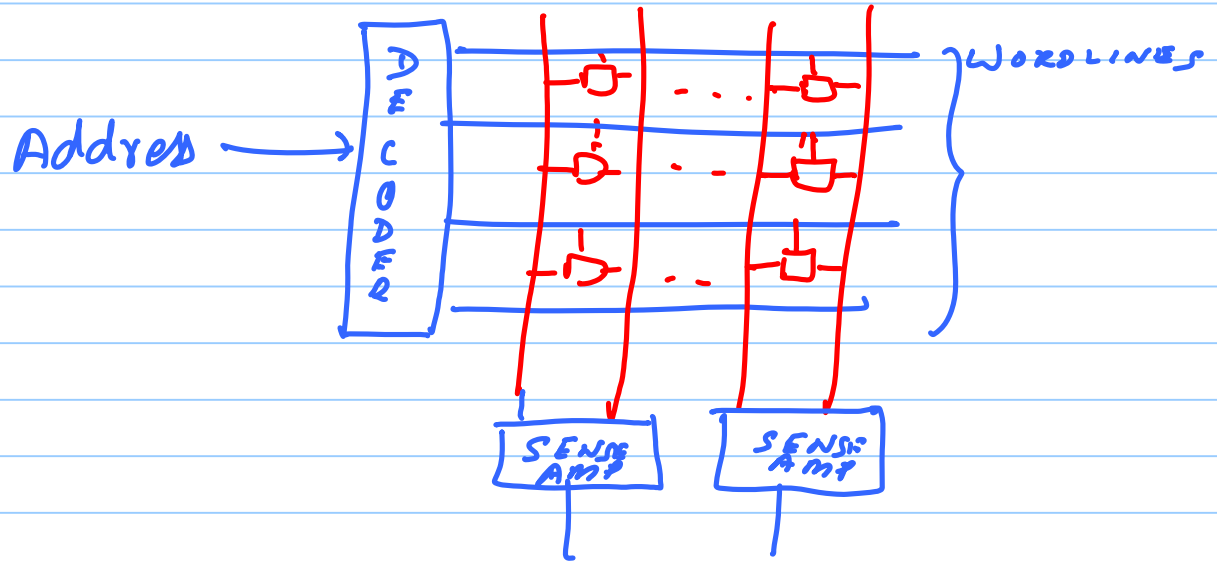
3) If $\Delta > T_p$

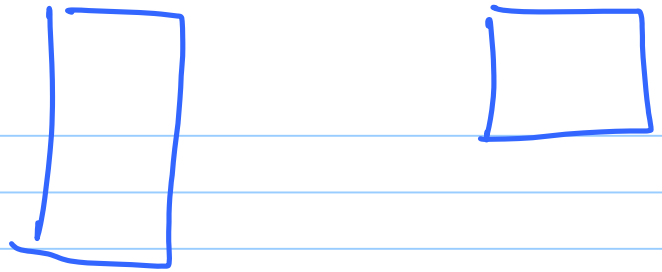
declare 1

$\Delta < T_N$

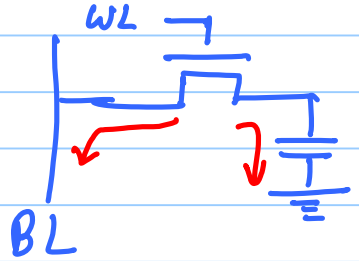
declare 0

SRAM ARRAY





1 TRANSISTOR CELL



DRAM CELL

Dynamic

✓ Very Dense

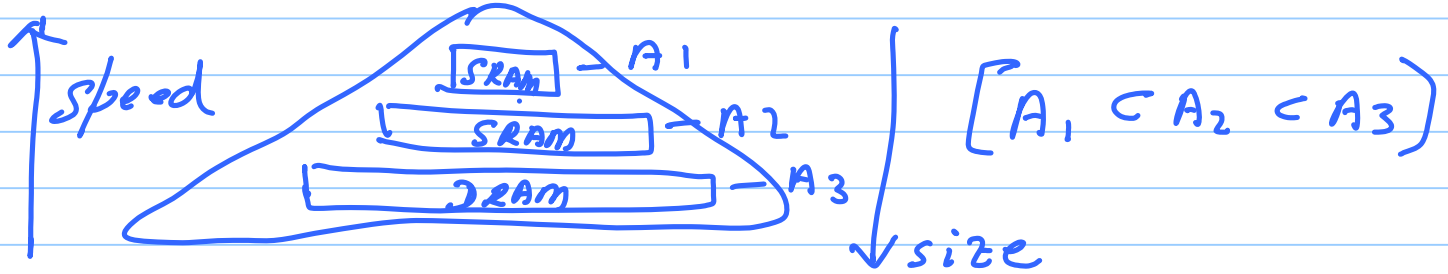
— Very Slow

— Periodically read/write all values (refresh)

	Speed	Density	Power	Use
Latch	+++	−	−−	[Registers & Pipeline regs]
SRAM	+	+	−	[Cache]
DRAM	−−−	++	++	[Main Memory]

What you know: One large array.

SW



$[A_1 \subset A_2 \subset A_3]$

Program behavior:

Saying: 90% of accesses come from 10% of locations

Temporal locality: Same data item is accessed frequently.

Spatial locality: If a data item, x, is accessed, then there is a high probability that another data item close to x is accessed in the same

window of time.

Hierarchy of Memory Systems