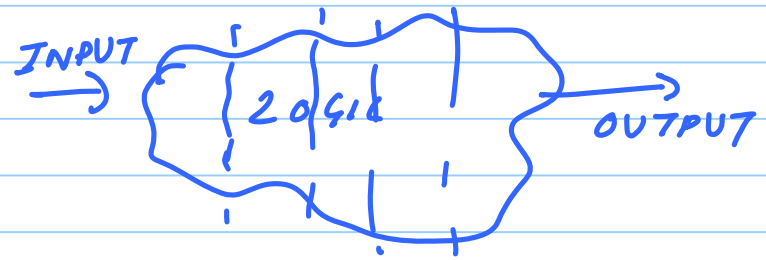
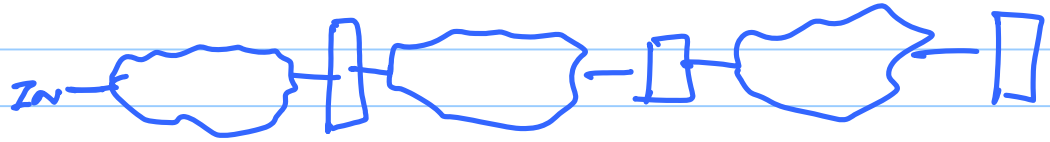
# Sep - 26

Note Title 26-09-2012








Pipeline Speed up:

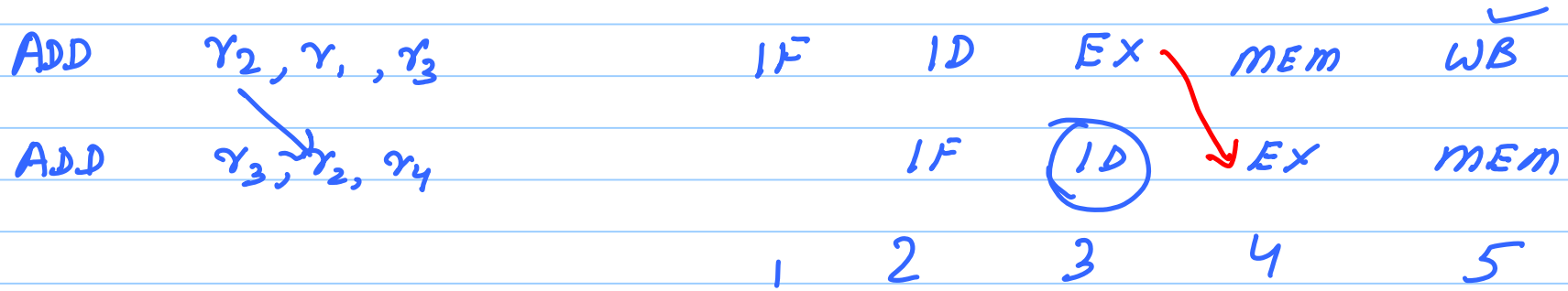
n insts (non-pipelined) : nk

(pipelined) : n + k - 1

Ex- $\text{Time}_{\text{ratio}} = \frac{n+k-1}{nk}$

$\text{Ratio}_{(n \to \infty)} = \frac{1}{k}$

| # insts. | ideal (0 latch delay) |
|---|---|
| 1 | $k$ |
| 2 | $k+1$ |
| . | |
| . | |
| $n$ | $n+k-1$ |


ADD r2, r1, r3
ADD r3, r2, r4
IF ID EX MEM WB
IF ID EX MEM
1 2 3 4 5

```
sw   r1, 20(r2)      IF   ID   Ex   MEM   WB
lw   r4, 20(r2)           IF   ID   Ex    MEM
```

forwarding / bypassing.

```
lw   r1, 20(r2)      IF   ID   Ex   M    WB
add  r3, r1, r4           IF   ID   Ex   M    WB
```

```
lw   r1, 20(r2)      IF   ID   Ex   M    WB
(bubble)   NOP            X    X    X    X    X
                          IF   ID   Ex   -
```

This pattern is known as a load-use hazard.

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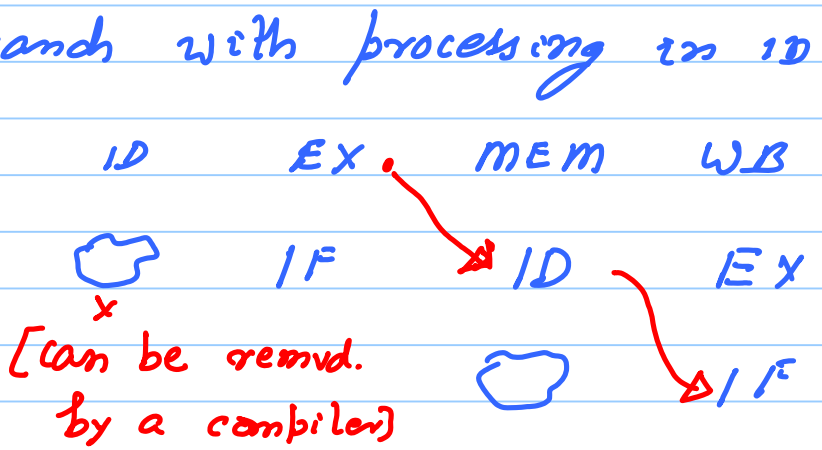
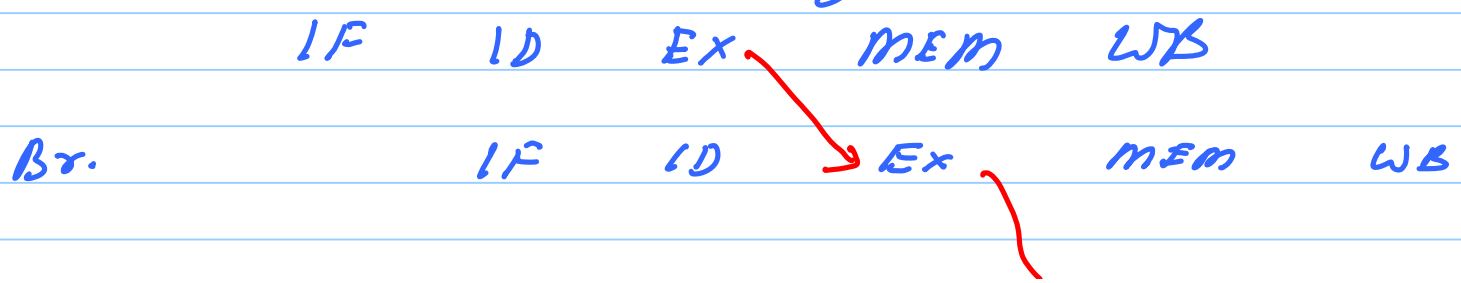
Control dependence

```
add  r1, r2, r3
beq  r4, r1, 20
```

Branch with processing in ID



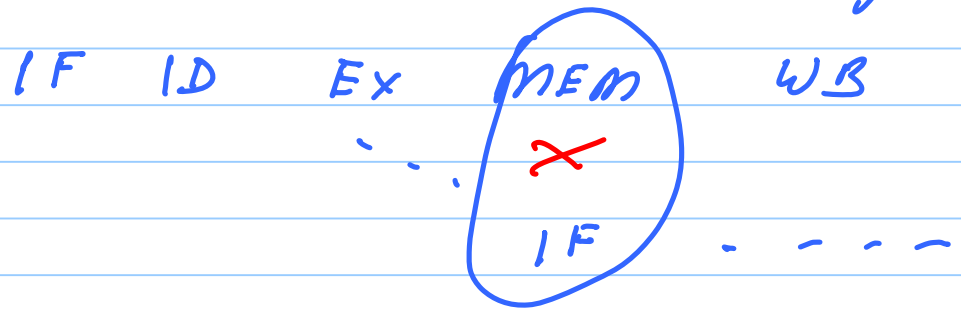

Branch with processing in Ex stage




## Structural Hazard

Assume that data and instruction mem are same.

You can satisfy one memory request per cycle.



Three kinds of pipeline hazards:

1) Data hazard (forwarding/bypass)
2) Control hazard (bubbling)
3) Structural hazard.