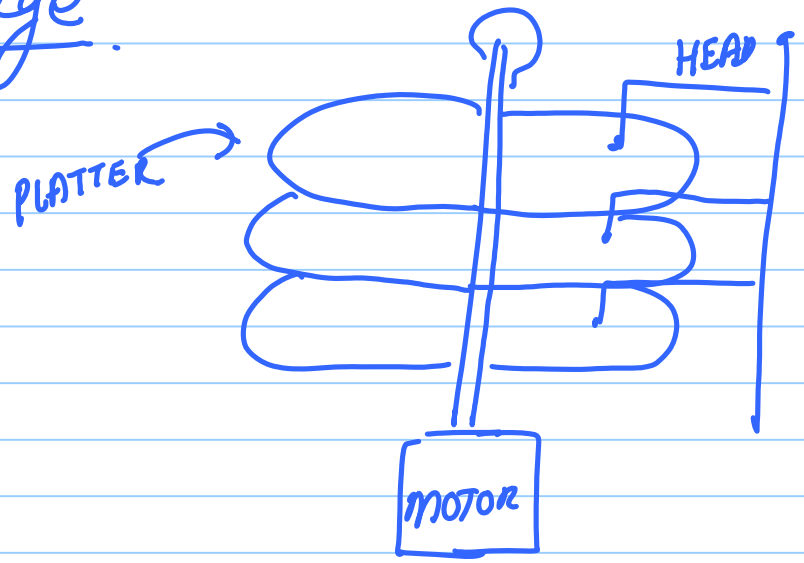
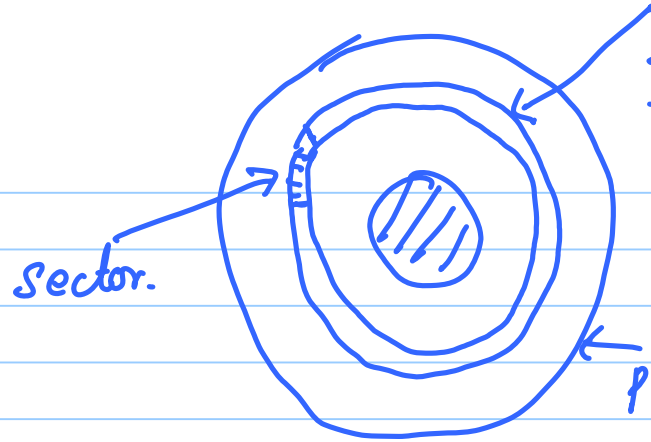
Nov 21

Note Title 21-11-2011

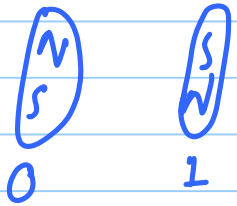
Come prepared with definitions of: bus, mesh ring, 2d torus 3d torus

Storage





Data is stored magnetically.



✗ Variable bit rate
: same no. of sectors / track

✓ Uniform bit rate
diff. number of sectors / track.

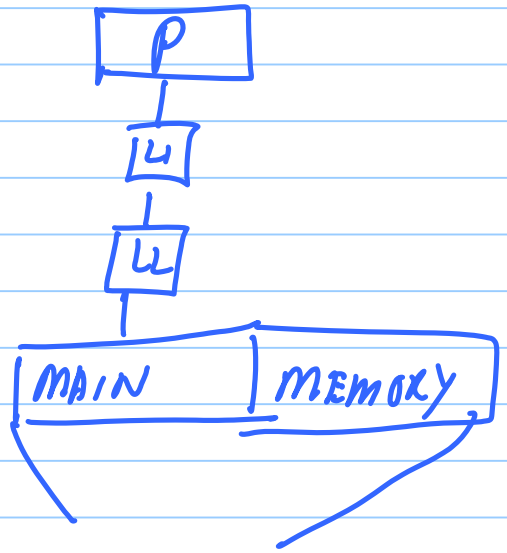
1. Move the head to the correct track (seek time)
2. Rotational Latency: Wait for the correct sector to come below the head
3. Bandwidth (data read/written per second)

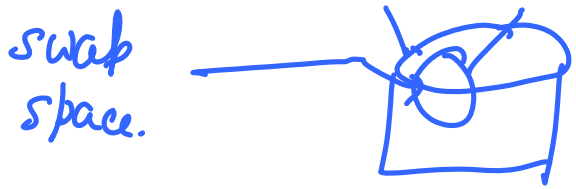
Total Latency of a disk access :

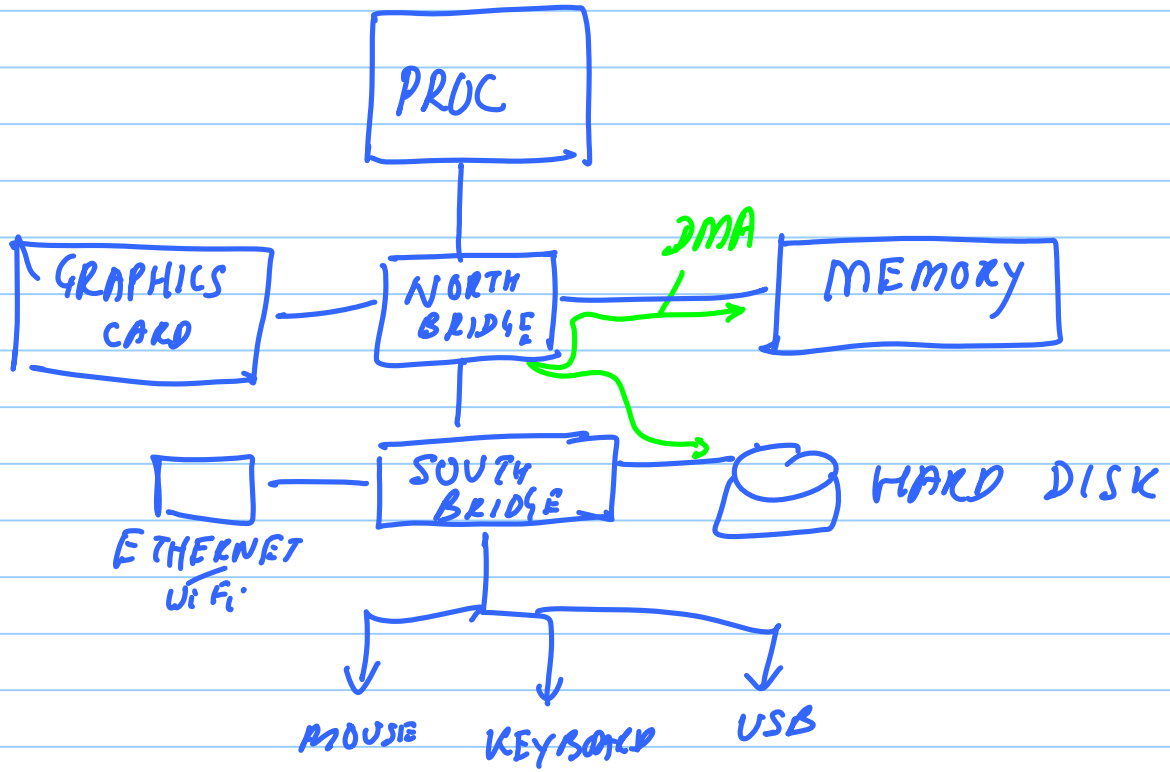
$$T_{seek\ time} + T_{rot\text{-}latency} + s/bw$$

$s \rightarrow$ data size

$bw \rightarrow$ bandwidth




swap
space.


PROC
GRAPHICS CARD
NORTH BRIDGE
DMA
MEMORY
SOUTH BRIDGE
HARD DISK
ETHERNET
Wi Fi
MOUSE
KEYBOARD
USB

Example

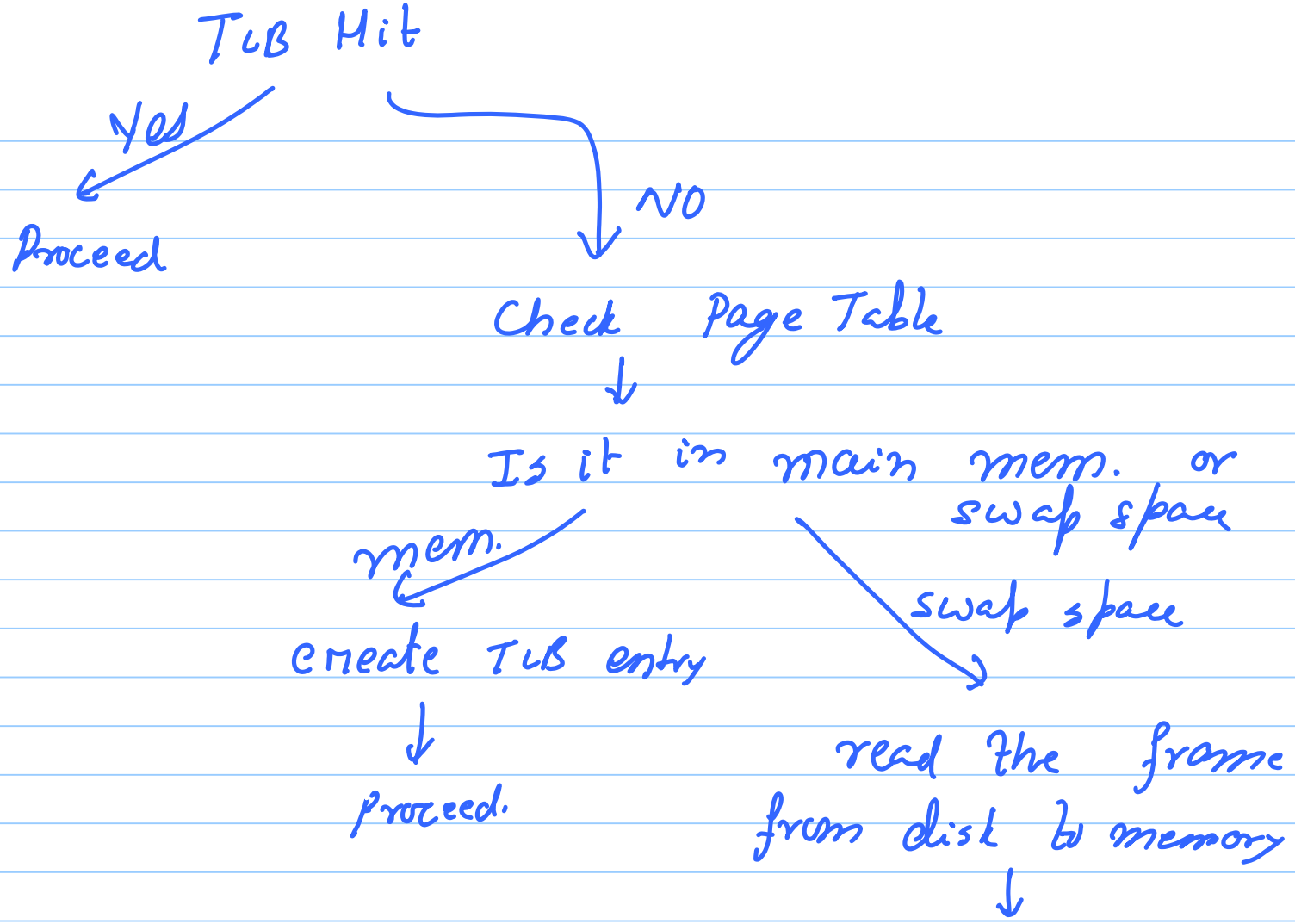
32 bit address space

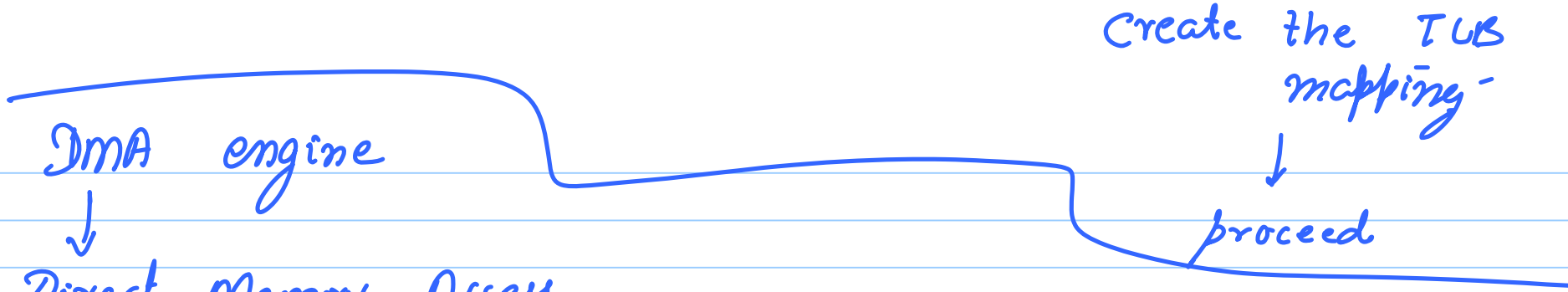
Virtual Memory: 4 GB

Main Memory: 256 MB

Game: 1 GB (memory footprint)

768 MB (HARD DISK SWAP SPACE) + 256 MB (main mem.)


TLB Hit
Yes
Proceed
NO
Check Page Table
Is it in main mem. or swap space
mem.
create TLB entry
Proceed.
swap space
read the frame from disk to memory



DMA engine

↓

Direct Memory Access.

(start addr. on disk, num-bytes)

↓

(addr in memory)

Once the DMA engine is done it sends an interrupt to the processor.

What happens to regular processor-memory traffic during a DMA transfer?

Burst Mode

DMA stops the processor.

Cycle Stealing Mode

Commercial Computer System

10^7 customers

Per customer: 100 MB

Total size: $10^7 \times 10^8$ bytes

= 1 PB

Reliability ↓↓

MTTF → Mean Time to Failure

MTTR → Mean Time to Recovery

Availability : $\frac{MTTF}{MTTF + MTTR.}$