Oct 4th.

Note Title 04-10-2011

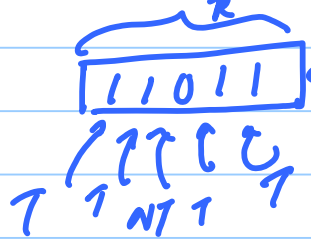
Branch Prediction:

1) Saturating Counter ✓

2) Bimodal ✓

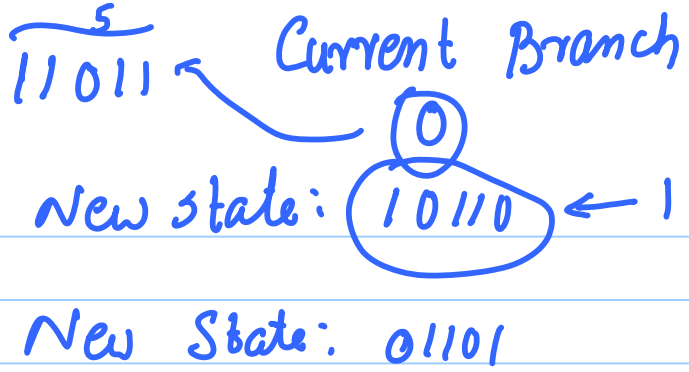
```
while (flag) {
    if (flag 2) ✓
        flag = 1;
    ---
}
```

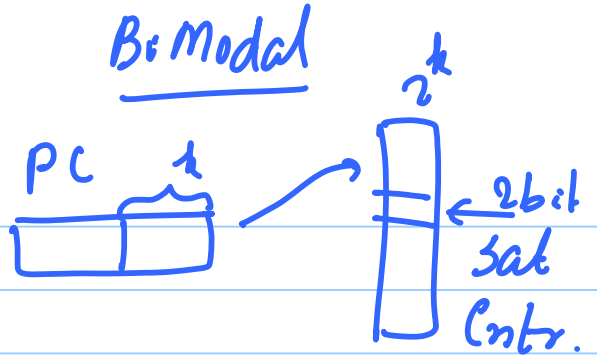
BHR (Branch History Reg.)



New Branch: NT

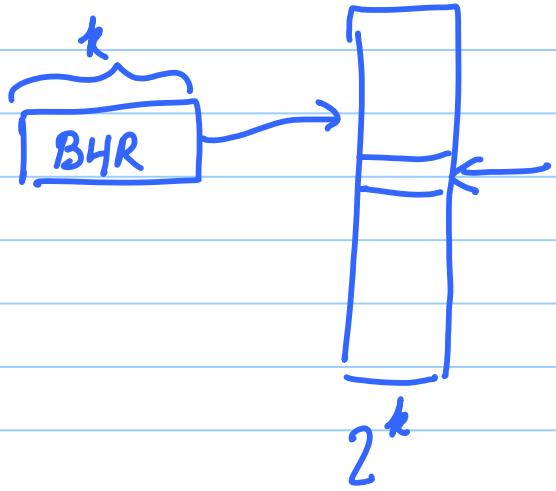
BHR = 10110





Correlating Predictors

Gag :

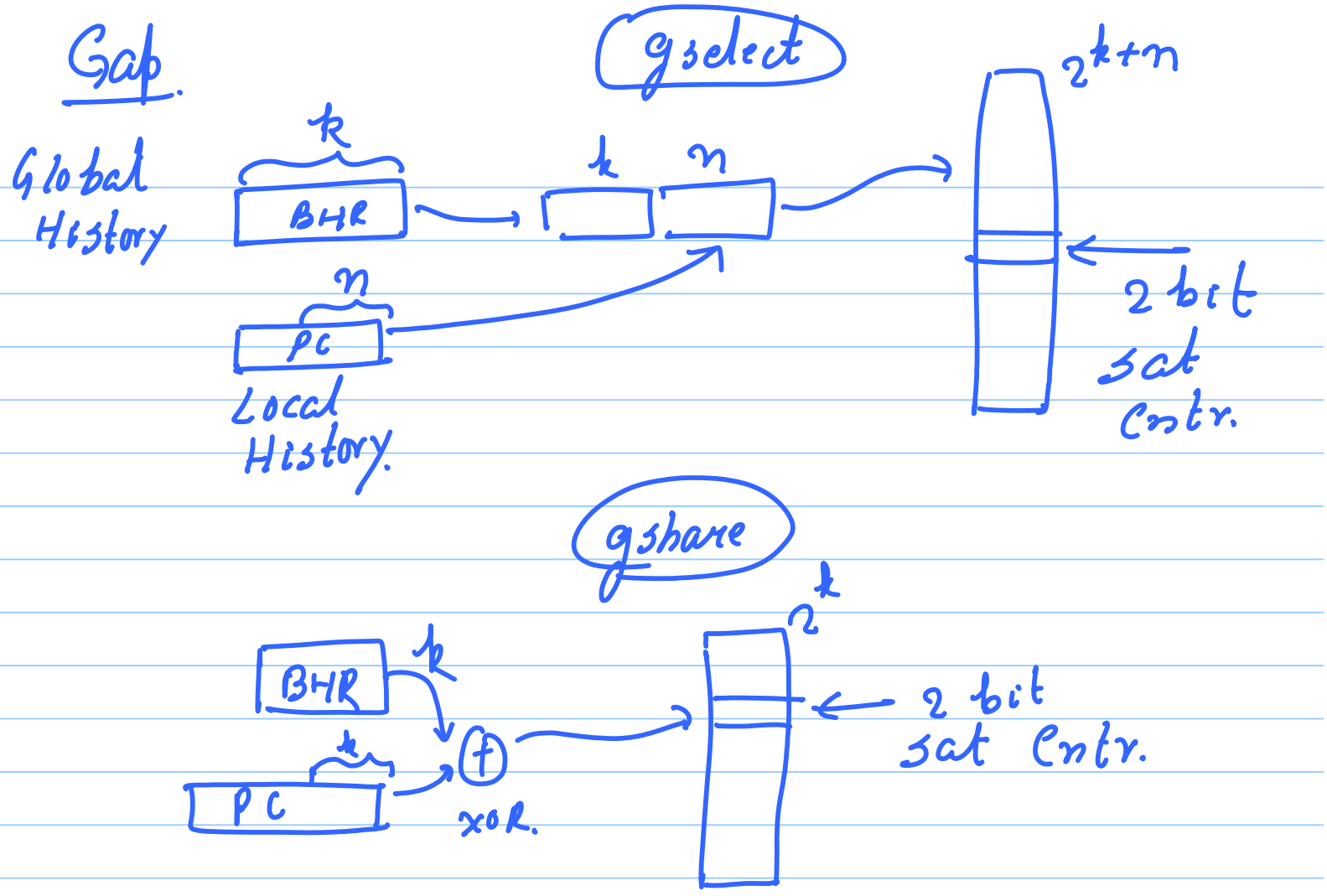


2 bit Sat. Cntr.

Let the value be v

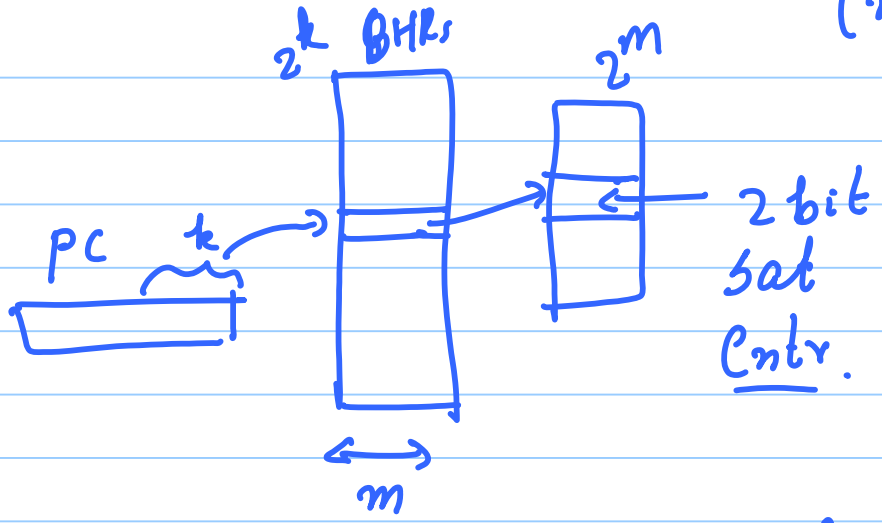
$v \in [0,1]$ (NT)

$v \in [2,3]$ (T)

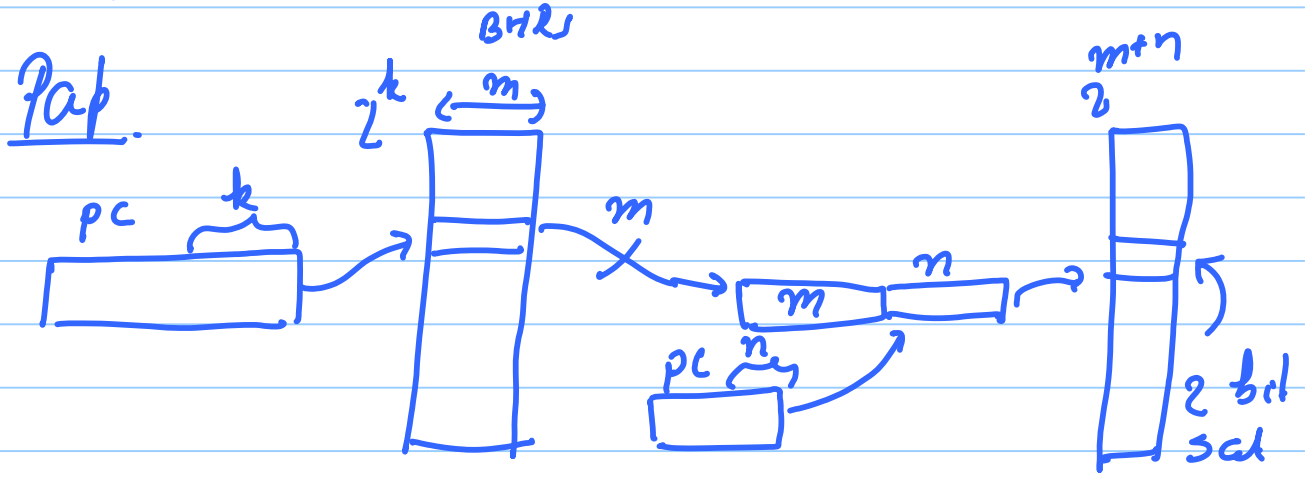

Gap
Global History
k
BHR
gselect
k
n
2^{k+n}
n
PC
Local History
2 bit sat Cntr.
gshare
2^k
k
BHR
k
PC
xor
2 bit sat Cntr.

Pag.

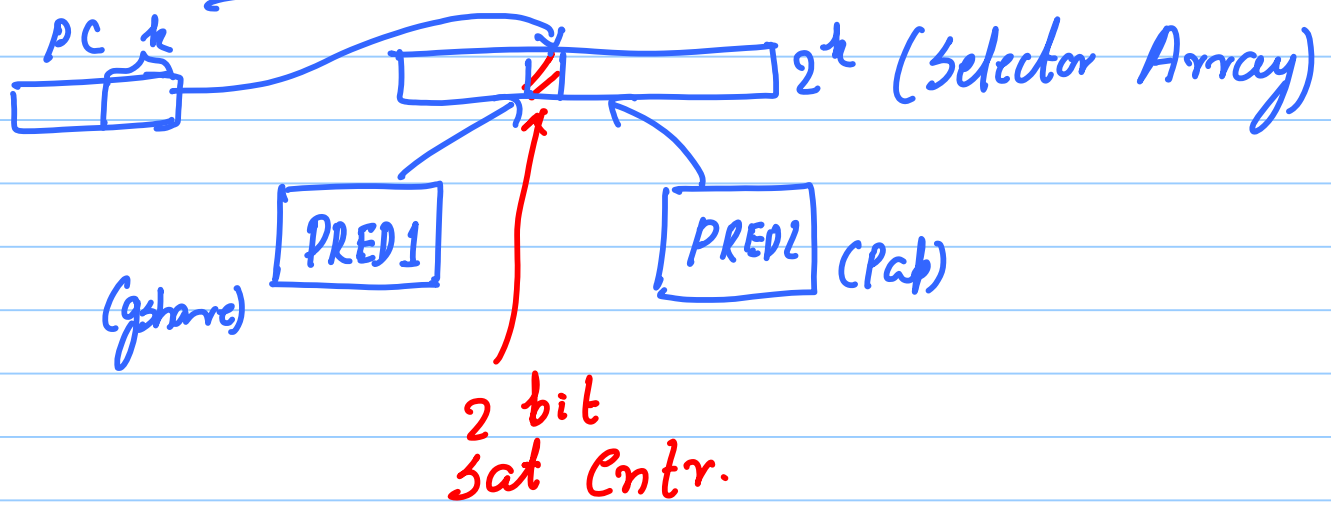
$(m \times 2^k + 2 \times 2^m)$



Pap.



Tournament Predictor



V → Value of 2 bit Sat. Counter.

Predict: $V \in \{0, 1\}$ Use Pred 1
$V \in \{2, 3\}$ Use Pred 2

Train: Both Correct OR Incorrect (do nothing)

Pred1 ✓	Pred1 ✗
Pred2 ✗	Pred2 ✓
√--	√++

Multiple Issue : (Pls. Read in the book).

1	IF	ID	EX	MEM	WB	
2	IF	ID	EX	MEM	WB	
3		IF	ID	EX	MEM	WB
4		IF	ID	EX	MEM	WB.

Support

1) Fetch: Ability to fetch 2 instructions (consecutive)

2) ID/RF: Extra resources

3) Ex: More : 2 ALUs

4) MEM: 2 ports

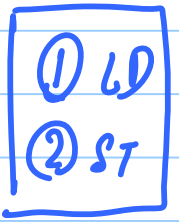
5) WB: 2 Reg. Write ports.

For 1 2 2:

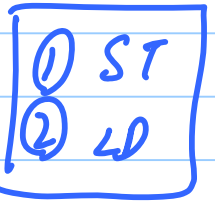
1) Compiler can schedule ∧ register dependences to eliminate between 1 2 2.

2) If it cannot make a 2-inst bundle insert no-ops.

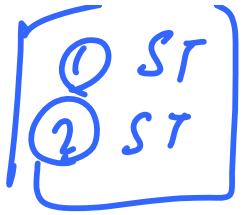
3) For a LD-ST case (trouble) can be detected after EX



stall ① → ②



Forward value to LD



x skip

4) Branch: Make Branch later. inst. of bundle