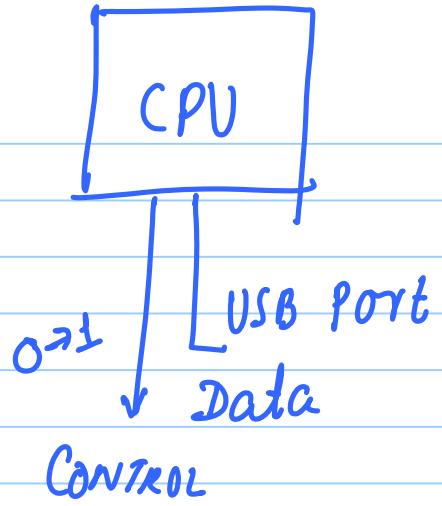
Note Title 11-10-2011

# Oct 11th

## Processor Pipeline Design

Exceptions:

- → Seg Fault
- → Page Fault (???)
- → Interrupt.




1) Interrupt

2) Finish WB

3) Flush Pipeline

4) Save PC of inst. in MEM stage

5) Load Interrupt handler

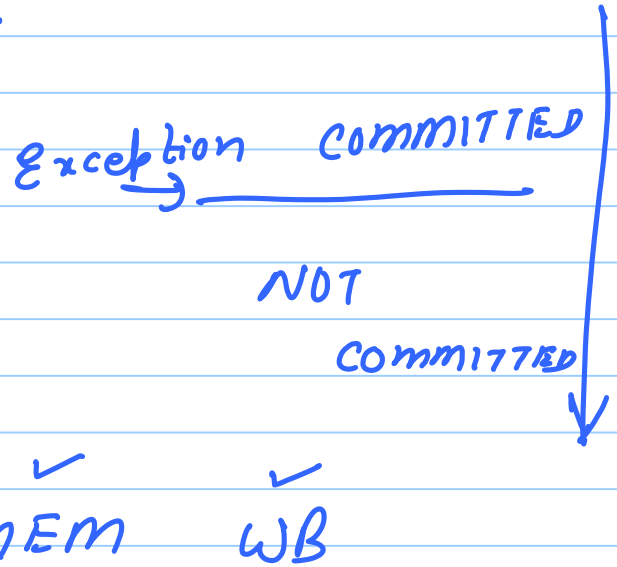
6) Save the registers

7) Process Interrupt

8) Clear Interrupt Request Line.

9) Reload the program
   - PC
   - Registers.

Precise Exception :



IF ID EX MEM WB

1) All exceptions/interrupts are flagged at the WB stage.

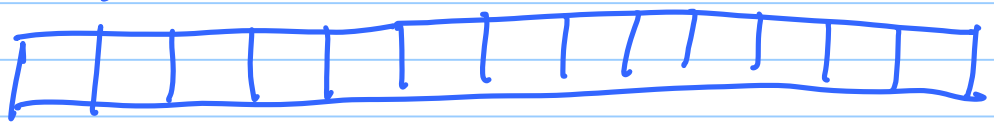
2) External Interrupt → Mute the mem stage.

3) Internal Exception → Do NOT make any changes till you reach WB stage.

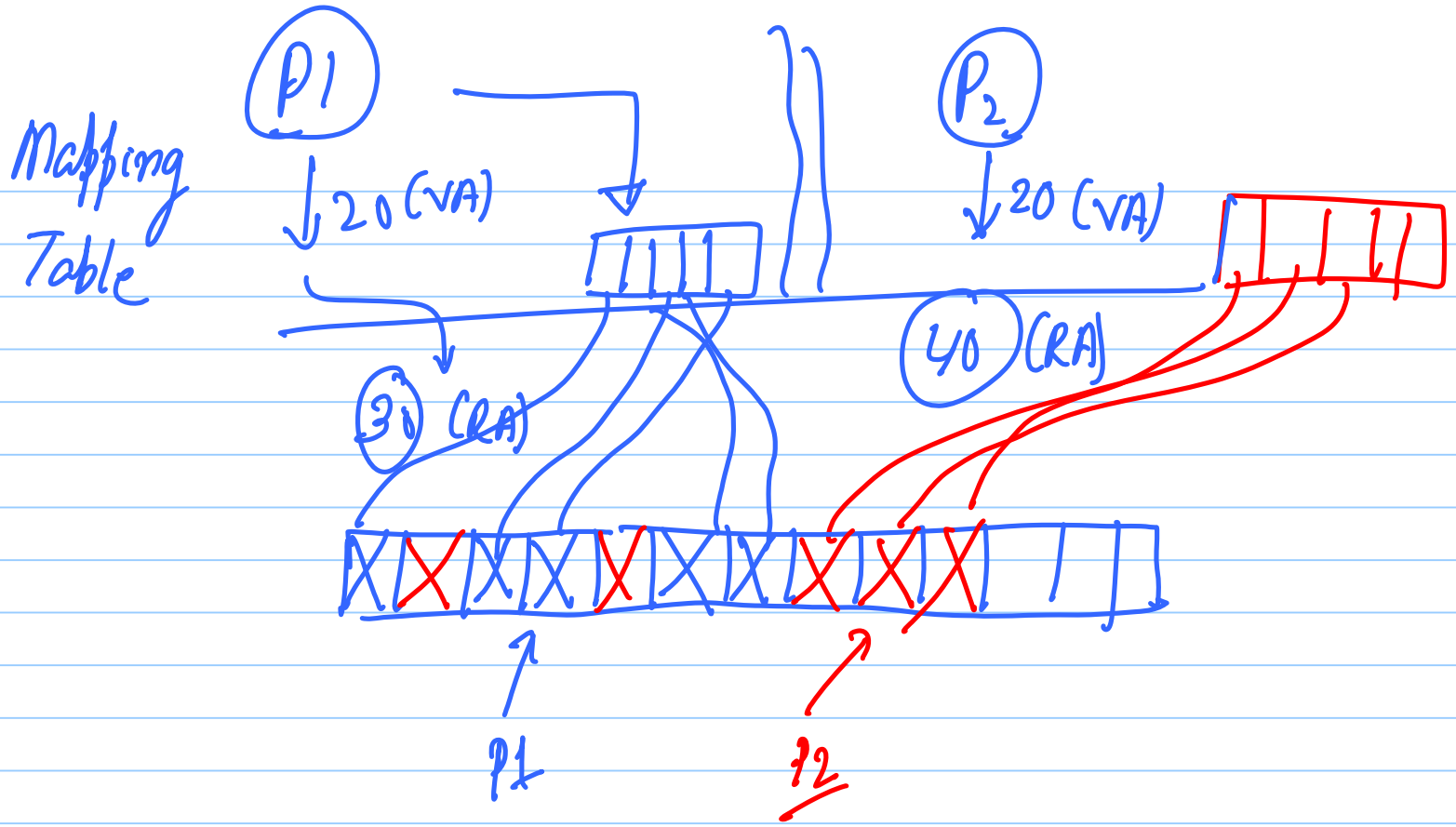
# Chapter 5.

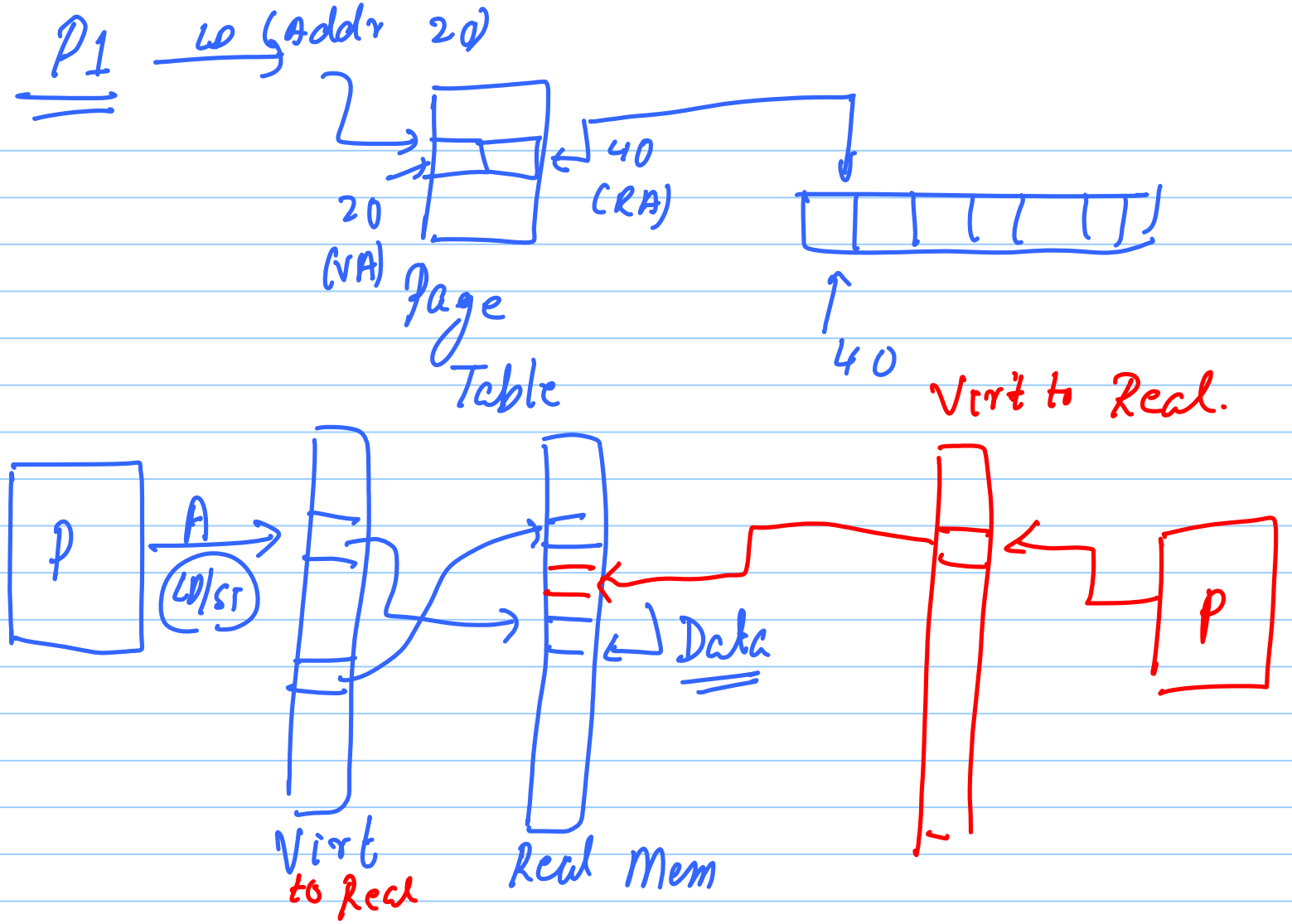
## Memory.

Our view of memory. (Virtual). One large array (private)



1) Insight:
   1) Virtual View of memory
   2) Usage per program: MB


P1
Mapping Table
20 (VA)
P2
20 (VA)
40 (RA)
30 (RA)
P1
P2


P1
LD (addr 20)
20
(VA)
40
(RA)
Page
Table
40
Virt to Real.
P
A
(LD/ST)
Data
Virt
to Real
Real Mem
P

page: 4 kB chunk in virtual memory

frame: 4 kB space in real memory.