Nov - 15th

Note Title 15-11-2011

FLASH

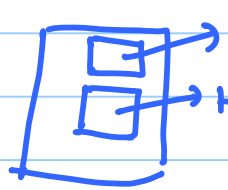
Floating Gate Transistor.

Read Operations: Very fast

Write Operations: → Very slow (10,000 × slower)

→ reliability is poor.

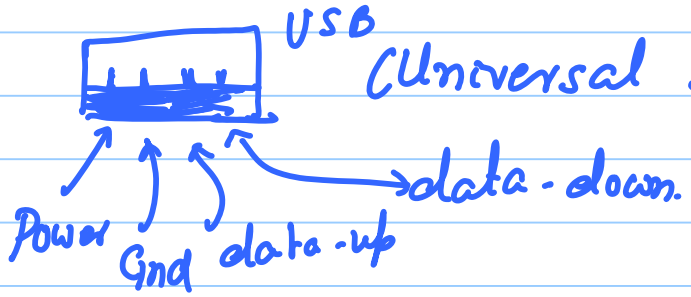
Wear levelling:



→ Not Used

→ Heavily Used

Wear Levelling → Keep changing the mapping of logical → physical blocks throughout. to minimize damage



Connecting Devices.

Mouse

Control

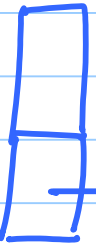
→ Interrupts.
- priority (masking).

→ Polling → ask individually.

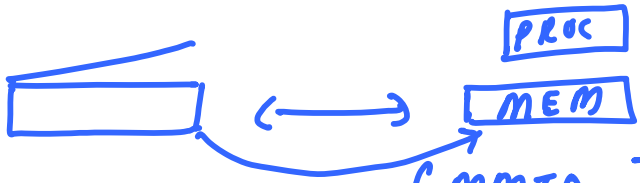
(x, y)

Data

→ Special I/O regs.



→ Memory Mapped I/O (mmIO)

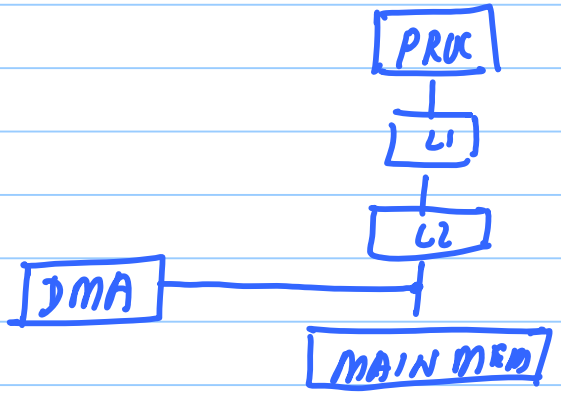


(MMIO TRANSFER)

DMA: Direct Memory Access

INPUT: < IO-DEVICE, NUM BYTES, MEMORY START ADDRESS)

DMA is done by a special DMA Controller chip.



① Bandwidth

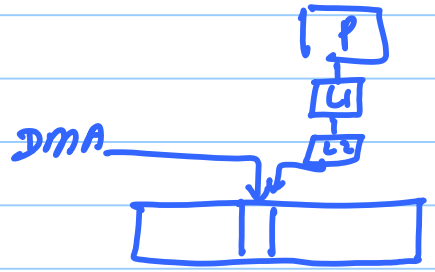
② Coherence

Bandwidth

1) Burst Mode (takes complete control)

2) Cycle Stealing Mode.

Coherence



INPUT INCOHERENCE PROBLEM

	Reg I/q	Mem Mapped I/O
Data	little	DMA
Control	∟	possible.

Reliability

MTTF (Mean Time to Failure)

MTTR (Mean Time to Recover)

Availability : $\frac{MTTF}{MTTF + MTTR}$

RAID : Redundant Array of Inexpensive Disks.

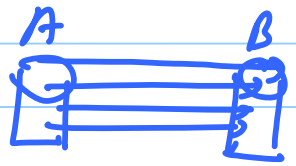
A B $C = A \oplus B$

RAID 0: No protection

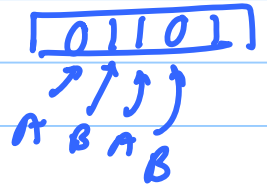
RAID 1: Mirroring

Two copies of data.

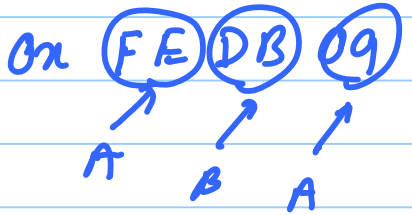
RAID 2: Parity at bit level



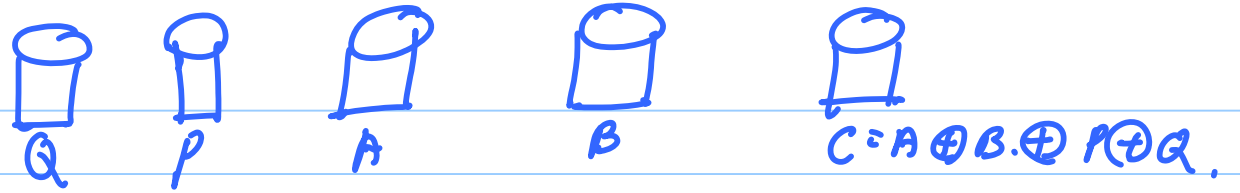
Parity Disk.



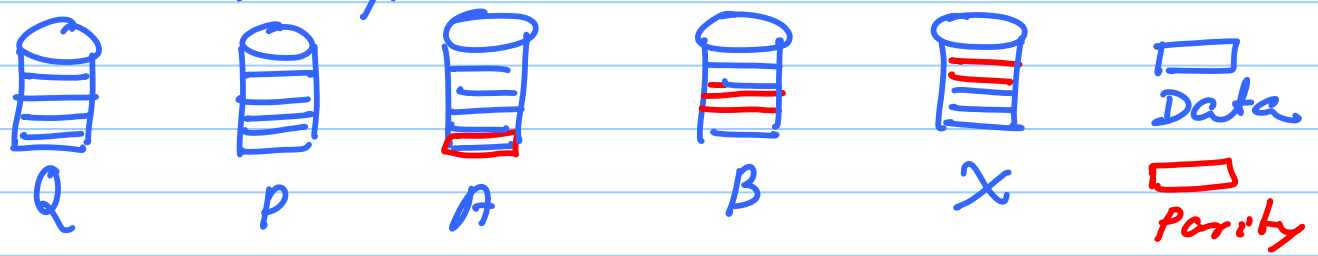
RAID 3: Parity at byte level



RAID 4: At a block level.



RAID 5: Distributed Parity.



RAID 6: Parity is contained in two disks.