Note Title 17-08-2011

$$\text{Yield} = \frac{1}{\left(1 + (\text{Defects per area} \times \text{Die Area}/2)\right)^2}$$

1) Performance
2) Power
3) Cost
4) Reliability

Performance : Wall clock time

$$\text{Performance} = \frac{1}{\text{time}}$$

Performance Equation.

$$P = \frac{\text{Program}}{\text{seconds}} = \frac{\text{Program}}{\#\text{ insts}} \times \frac{\#\text{ insts}}{\#\text{ cycles}} \times \frac{\#\text{ cycles}}{\#\text{ seconds}}$$

$$P = \frac{\underbrace{IPC}_{} \times f}{\#\text{ insts}}$$

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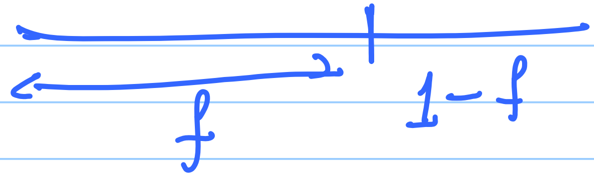
\# insts : ISA
Compiler

IPC : Organization of the processor

$f \rightarrow$ transistor technology
internal stuff.

Amdahl's Law



speedup : s

$$T = f + \frac{(1-f)}{s}$$

$$P = \frac{1}{f + \frac{1-f}{s}}$$

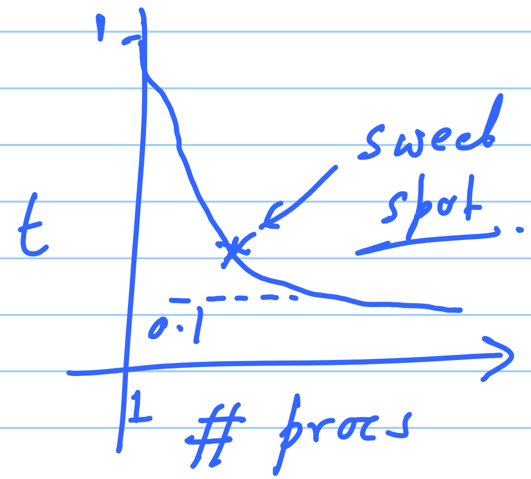
Parallel Program: Matrix Multiplication

s: 10% p: 90%

$t = 0.1 + \frac{0.9}{10} = 0.19$ } 10

$t = 0.1 + \frac{0.9}{100} = 0.109$ } 100

$t = 0.1 + \frac{0.9}{1000} = 0.1009$ }



2) Power → Dynamic (50%) $\propto CV^2f$

→ Static or Leakage Power (50%) $\propto T^2 e^{-V/V_T}$

[C → Gate capacitance
V → Vdd
f → frequency]

$V_T = \frac{kT}{q}$

k → Boltzmann Constant

q → 1.6×10^{-19} C

Mobile → 1W

Laptop → 50W

Desktop → 70W

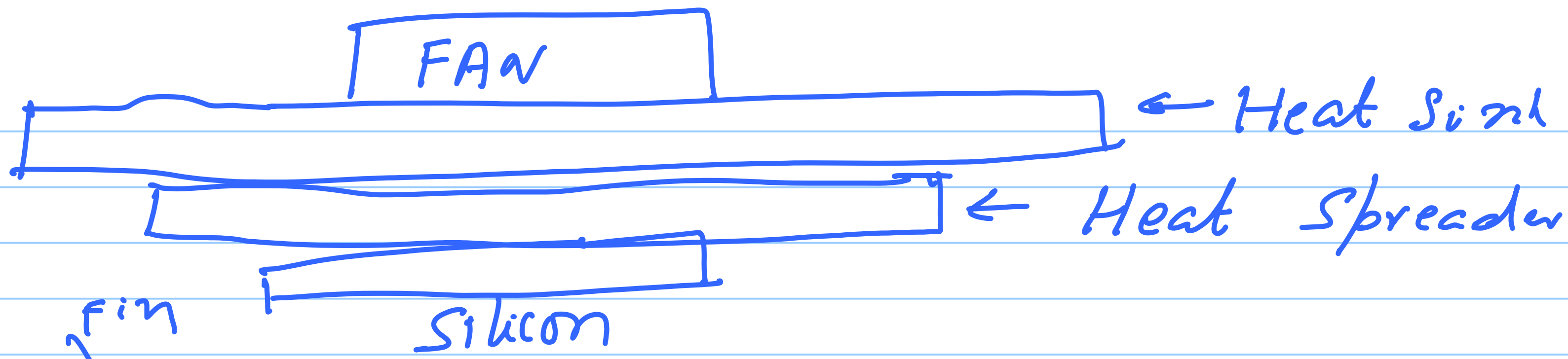
Server → 120W

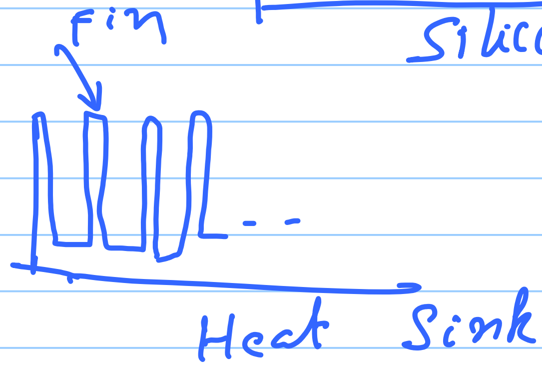
Super Server → 150W

Temperature

Mobile – 40°C
Laptop – 60°C
Desktops – 70°C

Servers: 100°C


FAN
Heat Sink
Heat Spreader
Silicon

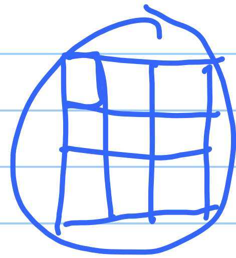

Fin
Heat Sink

Cost:

Moore's Law: Number of transistors on a chip would double every two year.

Size of a transistor decreases by $\sqrt{2}$.

180 nm → 130 → 90 → 65 → 45 → 32 → 22



Wafer

$$\text{Cost} \propto \frac{\text{cost per wafer.}}{\text{\# dies in a wafer} \times \text{yield rate}}$$

Reliability

1995 - Pentium I

1/2 billion dollars

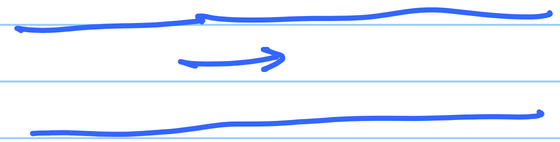
Soft Errors: Cosmic Rays

→ Alpha particles

→ Neutrons

Hard Errors – Wear & tear

Electromigration



Hard Error rates

$\propto e^T$